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ELEKTOR ELECTRONICS

37 IC ADDRESS

THE INTERNATIONAL ELECTRONICS MAGAZINE
JANUARY 1993
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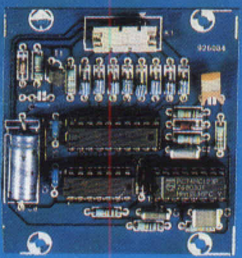
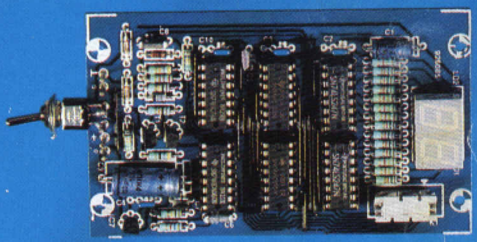
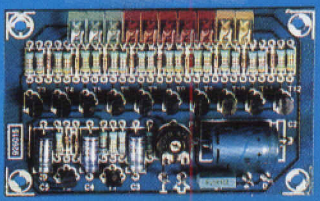
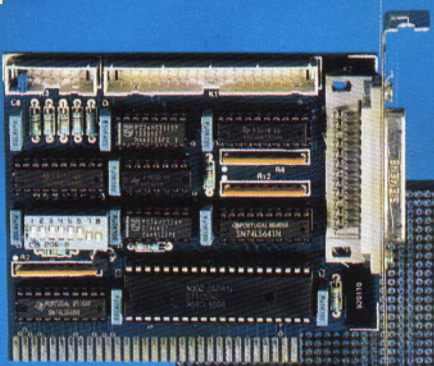
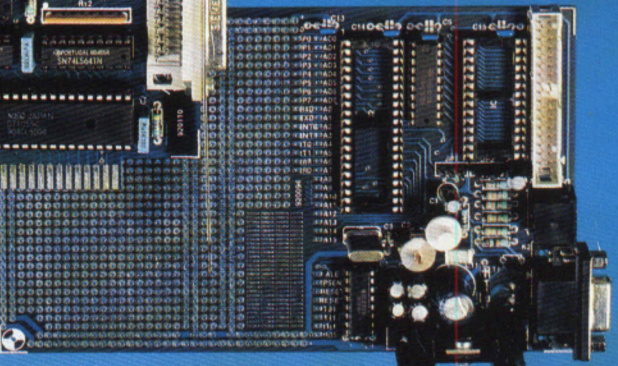
New series: Figuring it out

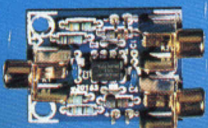


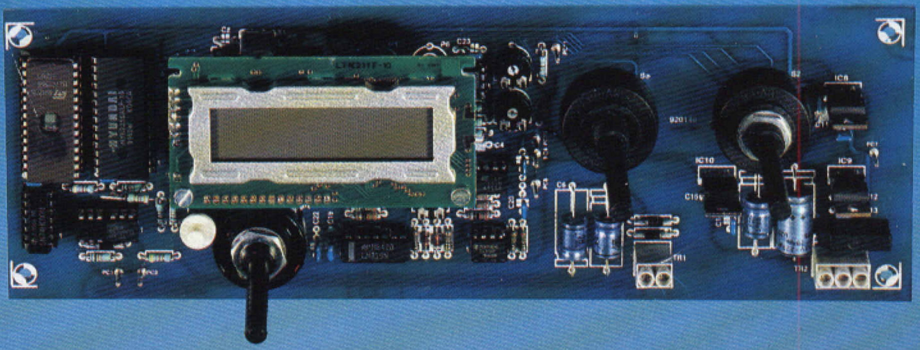












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ELEKTOR ELECTRONICS

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Volume 19
Number 207

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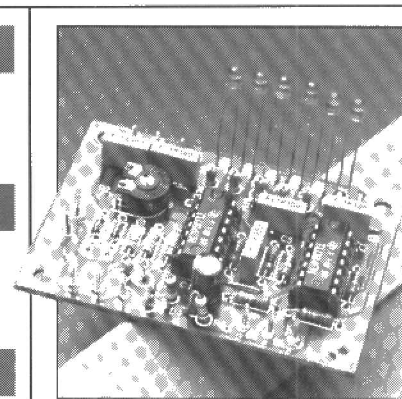

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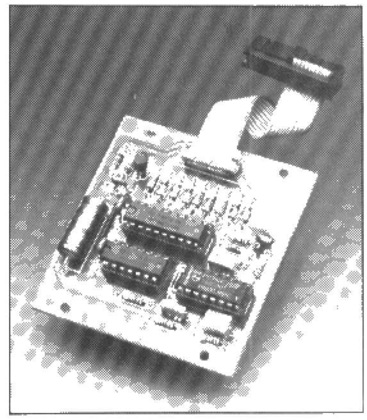

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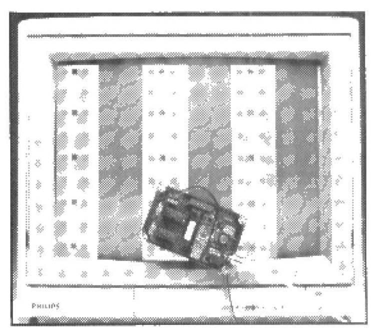

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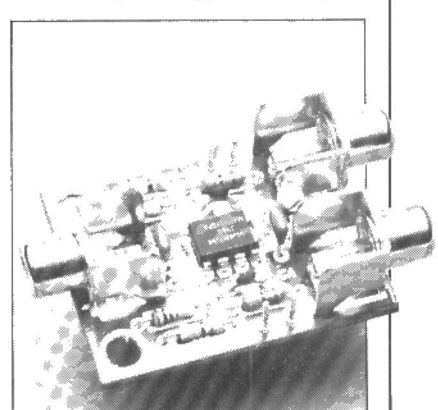


Dual video amplifier – p. 36

Front cover

Shown on this, the first of the New Year's issues, are some projects of today and some of tomorrow. Today's projects include the multicore cable tester (two units at the top) which can be found on p.20 of this issue and the dual video amplifier (second from the bottom at the left) which can be found on p.36. The unit at the bottom is the 80535 power meter which is planned for next month. Also seen are an LED VU based on standard ICs, an 80X32 development system and a 'PC recycling' insertion card. All of these projects are intended to be published within the next few months.

ELECTRONICS SCENE

UK FAILING TO EXPLOIT ITS TECHNICAL KNOW-HOW

In his inaugural address, Professor Peter Lawrenson, FRS, the 1993 president of the Institution of Electrical Engineers (IEE), Europe's largest professional engineering society, said that although it has long regarded itself as a nation of inventors, the UK is significantly failing to exploit its own technical know-how and expertise. It is also failing to recognize the importance of buying in the best know-how technology from elsewhere, and as a result is lagging behind its overseas competitors.

World trade in technical know-how, or disembodied technology, now amounts to $34 billion a year—more than the total of all international passenger fares—and is set to increase. However, Professor Lawrenson warned, this trade is increasingly being exploited by the USA, Japan and Germany.

"Although the UK", he said, "has always given rather 'mystical' prestige to inventions and patents, it has failed to award similar prestige to innovative success following from patents and the exploitation of knowledge through design rights, copyrights, trademarks and licensing".

"For too long we have suffered from a belief that cleverness in technology, and particularly science, is the key to success. Rather it is the exploitation of technical know-how and innovation that leads to the creation of benefit and wealth".

"The emphasis being placed internationally on knowledge and innovation, technology property and technology licensing has increased significantly within the past decade. Furthermore, there is a close correlation between those countries with high and increasing patent activity and those achieving industrial success. Against this background, the performance of the UK is disappointing, at the very least".

"The percentage of patents granted in the USA to UK inventors shows a steady decline whereas those of our main competitors, Germany and Japan, show a significant increase, reflecting the importance being attached in those countries to new technical knowledge".

"Some companies (in the UK) do have a positive attitude to patenting and to know-how transactions, including buying-in from outside, and are aware of the need to stay continuously abreast of worldwide best practice. Unfortunately, however, far too many companies seem to have no policy whatever in relation tot patenting or licensing strategy".

Professor Lawrenson ended his address with a call for a change in UK attitudes and for a new framework for positive action.

"There is a clear need for the implementation of vigorous policies to encourage the exploitation of know-how and technology, both by purchase and sale, to ensure that our manufactured products are truly of world-class design and quality and that every possible compensation is made for high labour and production costs and for restricted R&D budgets".

The Institution of Electrical Engineers, Savoy Place, London WC2R 0BL.

THE 16th EDITION BY OPEN LEARNING

The Open College, in collaboration with the IEEIE has developed an open learning course on the 16th Edition of the IEE Wiring Regulations. This course covers the scope and status of the Regulations and highlights the main requirements. It is intended for specifiers, designers, installers, and all who need a good working knowledge of the Regulations.

The open learning approach, which has proved so successful with the Institution's Mathematics for Engineers and Technicians programme, will particularly appeal to those unable to take time away from their work, since its flexibility enables study to be carried out at a time and place convenient to the learner.

The Institution of Electronics and Electrical Incorporated Engineers, Savoy Hill House, Savoy Hill, London WC2R 0BS.

LOW COST DATA LOGGER

Pico Technology have added the ADC-16 to their range of PC-based data acquisition products. This is a high resolution data logger that plugs directly into the serial port, requiring no external power. It provides eight channels of analog input at 16-bit (plus sign) resolution.

Unlike plug-in cards, it uses no expansion slots, which makes it easy to install and ideal for use with portable PCs. The use of a serial connection cable means the unit can be positioned near the experiment to minimize noise pick up.

It is supplied with PicoLog data logging software that allows full use of the ADC-16's features: you can select the resolution for each channel from eight to 16 bits and either single-ended or differential inputs. Each recorded sample can be the maximum, minimum or average of a number of readings, collected over a period of a few milliseconds to a day. The software also includes a comprehensive range of graphical and text reporting tools.

The ADC-16 costs £99 (plus VAT) which includes software drivers and a manual.

Pico Technology Ltd, 149-151 St Neots Road, Hardwick, Cambs. CB3 7QJ.

EMBEDDED CONTROLLER BULLETIN BOARD

An electronic Bulletin Board Information service has recently been opened by Hitex (UK), claimed to be Europe's foremost manufacturer of in-circuit emulation equipment. The board contains up-to-date information on microcontrollers and development tools and is a valuable source of information for embedded system programmers.

The board is host to a wide range of conferences covering most of today' most popular microcontrollers and programming languages, and is also home to the C51 and C166 user groups for the popular 8051 and Siemens SAB80C166.

In addition, there is a wide range of real applications and demonstration software available for downloading free of charge, along with a comprehensive library of technical articles which can be read on-line or downloaded for printing.

The board is open from 8.00 am to 9.30 pm Monday to Saturday. membership is free and there is no charge for time spent on the system. Log on to the board by dialling (0203) 690 026 and connecting at any standard baud rate up to 2400 with eight bits no parity one stop bit.

Hitex (UK) Ltd, Sir William Lyons Road, Science Park, Coventry CV4 7EZ.

MAPLIN IN SOUTHERN AFRICA

Maplin Electronics have established their services in southern Africa as part of a continual expansion programme, which has seen its UK retail outlets increase to 19, the opening of a custom-built, high-tech distribution warehouse and the award of the BS5750 Certificate of Quality. The new set-up aims to provide both the hobbyist and the professional the same fast, efficient, value-for-money service as has been provided in the UK for the past 18 years.

Mr Roger Allen, Maplin's Managing Director, explains the move: "There are some 9000 British electronics magazines distributed each month in southern Africa, but their readers face difficulties in sourcing suitable components and hardware to complete the projects that these magazines publish. Maplin (South Africa) aims to overcome these problems and has distributed 10 000 southern African editions of the 1993 catalogue throughout South Africa, Namibia, Botswana, Lesotho and Swaziland".

The southern African edition of the Maplin catalogue includes a Rand price supplement

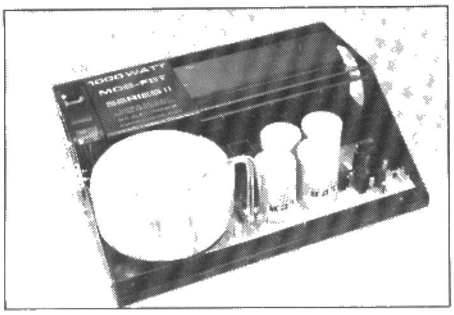
as well as details of how to order goods from the new service.

Maplin (South Africa) Ltd will be headed by Mr Hans Moeller, who has over 25 years experience in the electronics and radio communications field in southern Africa. The phone and fax number of the new office are 24 511 603 and 24 512 507 respectively.

Maplin Electronics PLC, P.O. Box 3, Rayleight SS6 8LR.

POWERFUL AF MODULE FROM BK

The new MOSFET amplifier module Type OMP/MF1000 from B.K. Electronics has double the power of the Type OMP/MF450, which it supersedes as the flagship of the OMP module range.



Delivering 1000 watts r.m.s. into a 2 Ω load, the OMP/MF1000 provides a no-compromise price/power/performance ratio and, as with all of the OMP range, its advanced MOSFET circuitry achieves superb sonic clarity with enduring reliability.

The OMP/MF1000 is priced at £259·00, incl. VAT, plus £12·50 delivery and is available from

B.K. Electronics, Units 1 & 5 Comet Way, Southend-on-Sea SS2 6TR.

PAN-EUROPEAN ENGINEERS?

A working group, led by the 28 000 strong Institution of Electronics and Electrical Incorporated Engineers (IEEIE) to investigate the feasibility of establishing pan-European courses for Incorporaed Engineers in electronic and electrical engineering, has made its final report to the European Community under the ERASMUS programme.

Reflecting opinions from within the twelve member states of the EC and five of the EFTA countries, the report acknowledges the important work done in achieving mutual recognition of qualifications and professional titles by the EC with its Directive on the Professions. It also deals with:

- the need for further investigation into the concept of a more practically oriented engineer involving within a truly European education and training framework;
- the features of European Incorporated Engineer courses in electronic and electrical engineering, with sections on entry to course, length of study, and a description of the areas of employment and activities of European Incorporated Engineers;
- the importance of work being done to compare different countries' engineering education systems, which have evolved naturally against different social, cultural and industrial backgrounds.

The working group, chaired by Barry Dobson, Head of Engineering, Science & Technology at North Hertfordshire College, and Chairman of the IEEIE's Academic Accreditation Committee, has not sought to define a new syllabus but primarily to identify features from existing courses against which European Incorporated Engineer courses can be assessed.

The IEEIE, Qualifications Dept, Savoy Hill House, Savoy Hill, London WC2R 0BS.

EUROPEAN STANDARDS ISSUES

European standards are a vital factor in the development of the single market and these standards must reflect the market's and users' requirements. A conference, 'Standards for Europe 1993 Onwards', a joint initiative of CEN, CENELEC and ETSI, the three standardization bodies, was held in November in Brussels to provide an opportunity for an open exchange of views between all interested parties – trade associations, professional bodies, consumer groups and large and small enterprises.

An important aim of the conference was to provide a link between the market's requirements for harmonized products and services and the European standardization process. Other issues covered by the conference include:

- Technical and political issues facing European standardization
- Harmonizing European requirements.
- Avoiding technical barriers to pan-European and worldwide trade.
- Conformance assessment of European products.
- Ensuring a greater freedom of choice for the consumer in a competitive market of harmonized products and services.
- Enabling customers/consumers to buy products and services of the right quality and price whatever their global origin.

CEN (European Committee for Standardization) is the association of the national standards bodies of 18 European countries (12 EC and 6 EFTA). Since 1992, CEN is also open to European organizations representing interested economic partners.

CENELEC (European Committee for Electrotechnical Standardization), owned by its members, is the vehicle whereby the lectrotechnical community in Europe generates standards and related agreements. It consists of the National Electrotechnical Committees of 18 EC and EFTA countries that bring together all the relevant interest at the national level and has recently widened its scope to take on board affiliates from eastern Europe.

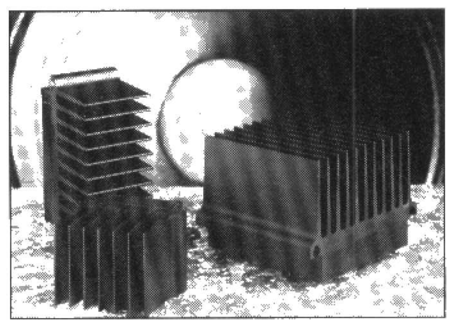
ETSI (The European Telecommunications Standards Institute) works as an open forum. Its task is to set uniform telecommunications standards for Europe that will be adopted by each individual country, thus linking national networks and services and ensuring interoperability of equipment. It draws on all interested parties: administrations, public network operators, manufacturers, users, service providers and research bodies. It is an independent, self-funding organization with a small permanent staff, but throughout Europe it has nearly 2000 technical experts working om specific technical projects.

ETSI, JPG Secretariat, Route des Lucioles, 06921 Sophia Antipolis Cedex, France.

ILP AF AMPLIFIER MODULES FROM CIRKIT

Cirkit Distribution is now stocking the complete range of ILP audio power amplifier modules. These modules provide a versatile range of building blocks for constructing high-quality audio amplifiers with the minimum of additional components. Applications range from low-power hi-fi-quality amplifiers to high-power stage amplifiers.

The modules are manufactured in three



types: bipolar, MOSFET and Class A. Each amplifier is encapsulated to an integral heatsink which, together withg internal protection, make these extremely rugged, both electronically and mechanically. With power ratings from 15 to 180 watts r.m.s, the amplifiers produce very low THD: in the MOSFET types less than 0.005%; the input sensitivity of these types is only 500 mV for full output.

Cirkit Distribution Ltd, Park Lane, Broxbourne EN10 7NQ.

NEW TV CHIPS

The trend in television technology is toward fewer chips per set and hence a reduction in costs. Siemens has developed a range of new ICs for this application field; TV designers who use them can also speed up development times, while further improving picture and sound quality.

There are two 3-band mixer/oscillator/IF driver ICs for terrestrial hyperband tuning, ref. TUA 2009X and TUA 2019X. Another mixer/oscillator IC is the MTI 3000X, which can be used to produce an inexpensive 2-band hyperband tuner.

The SDA 3352X is a 1.3 GHz PLL chip for automatic tuner alignment.

The TDA 6812-2 stereo decoder for TV sets offers a very high signal-to-noise ratio of over 85 dB.

The TDA 6050 video/sound IF amplifier will put an end to the frequent missing of whole lines of videotext on current TV sets.

The TDA 5940 and TDA 5950 video/sound IF combined amplifiers process the sound and picture IF on a single chip. The TDA 5940 is designed for PAL applications, while the TDA 5950 is designed for multi-standard equipment.

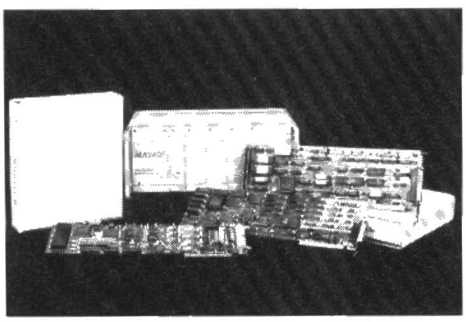
Siemens Ltd, Siemens House, Windmill Road, Sunbury-on-Thames TW16 8HS, England

POWERFUL DATA ACQUISITION ON A PERSONAL COMPUTER

Cambridge Research Systems has developed a software package, named CAOS for use in conjunction with its range of processor-controlled data-acquisition cards. Compared with other programming aids for intelligent cards, its operation is not limited by inbuilt commands or functions.

CAOS can be used with any of CRS's range of IBM-PC compatible systems. Consisting of an extensive library of 'C' and Pascal functions for the capture and processing of data, it eliminates the need to learn any other computer languages.

With CAOS, data, organized in buffers, may be manipulated through the use of functions such as filtering, computing fast-Fourier transforms (FFT) and calculating statistical information. Full support is provided for such high-level operations as direct screen input/output, and the transfer of data to and from the PC.



The combination of CAOS programs and programmable data-acquisition cards provides the user with the ability to create applications that can be downloaded from the host computer and run autonomously, simply transferring data back to the PC at convenient intervals. By removing the need for the host computer to service the card in real time, the system is ideally suited for use with non-real-time operating systems like Unix and Microsoft Windows.

Cambridge Research Systems Ltd, 80 Riverside Estate, Sir Thomas Longley Road, Rochester ME2 4BH, England.

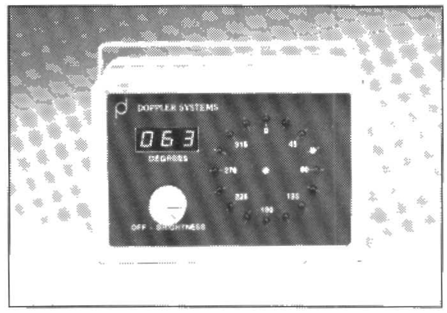
NEW RADIO DIRECTION FINDERS

Tony Chapman Electronics have launched the new Doppler Systems Inc. series of Radio Direction Finding Systems in the UK. The 5000 series provides a wide frequency coverage from 100 MHz to 1000 MHz.

The system consists of a processor and a control unit with bearings being displayed via a high-intensity LED 'ring of lights', as well as three-digit bearing information. Options include an RS232 serial interface and a speech synthesizer and a loudspeaker that enunciates the bearing every 2.1 seconds.

A number of combinations are available for the antenna, which may be either mast or magnet mounted, allowing fixed or mobile applications. The direction finder system may be integrated with AM and FM scanners or fixed receiver.

General specifications of the direction finder include quasi-Doppler 4-element antennas; commutation 300 Hz; frequency range



100–1000 MH; accuracy ±5%.

Tony Chapman Electronics Ltd, Electron House, Hemnall Street, Epping CM16 4LS, England.

NEW FILTER MODULES FROM KEMO

Intended for data-acquisition applications, where high performance has to be combined with high component density, the new 1600 series of filter modules from Kemo offers significant benefits compared with IC filters. The new modules offer cut-off frequencies of up to 51 kHz and down to 2 Hz.

Continuous time filter techniques mean that the modules suffer from none of the problems that limit the use of single-chip IC filters: there is no excessive variation of DC off-set with cut-off frequency, and no high-frequency clock breakthrough or input aliasing. Noise and linearity are also far superior, and allow the filters to be used with convertor systems of the highest performance.

The 1600 series modules can be supplied with a wide range of filter types and response shapes, including low-pass for high-performance alias protection, high-pass for the elimination of low-frequency disturbances prior to conversion, and special-purpose responses including band-pass and band-stop.

Kemo Ltd, 9–12 Goodwood Parade, Elmers End, Beckenham BR3 3QZ, England.

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Editor/publisher: Len Seymour
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Editorial & Administrative Offices:
P.O. Box 1414
DORCHESTER DT2 8YH
England
Telephone: (0305) 250 995 (*National*)
or +44 305 250 995 (*International*)
Fax: (0305) 250 996 (*National*)
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Head Office:
P.O. Box 75
6190 AB BEEK
The Netherlands
Telephone: +31 46 38 94 44
Telex: 56617 (elekt nl)
Fax: +31 46 37 01 61
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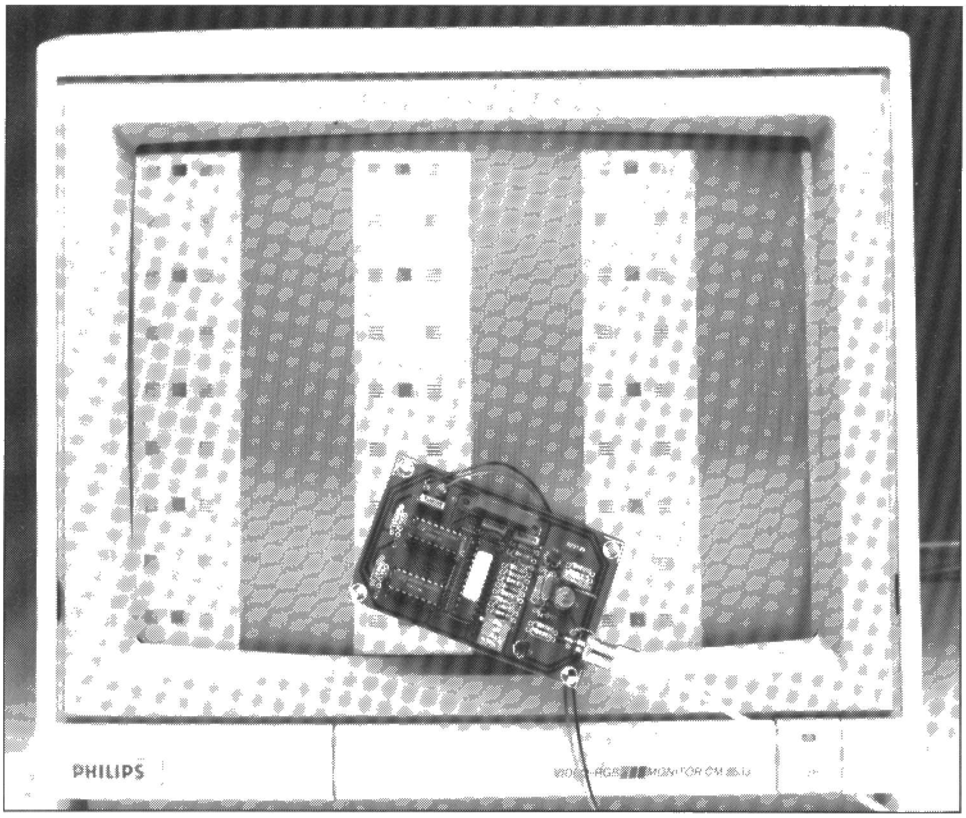
PAL TEST PATTERN GENERATOR



BRIEF SPECIFICATION

- **Quartz controlled for optimum stability**
- **Four test patterns:**
  - **- green (225°)**
  - **- orange (134°)**
  - **- green with 4 white bars**
  - **- orange with 4 white bars**
- **Based on readily available components**
- **Simple to adjust**
- **Compact design using one GAL**
- **Digital RGB-csync outputs**

A stable reference signal is essential whenever you want to adjust a television or a video monitor. Special integrated circuits have been developed that enable a PAL/NTSC colour test pattern generator to be built from a minimum of components. Unfortunately, these ICs are generally expensive as well as hard to obtain, and that is why we propose to do without one for a change.

Design by W. Foede

A number of PAL test chart generators were published in this magazine over the past few years. These circuits are generally based on integrated PAL encoder ICs to ensure that all synchronization signals are correctly timed. The entire sync processor is thus contained inside a single IC, which affords good repeatability of a circuit for home construction.

The test pattern generator described here is based on remarkably few components: two digital counters Type HC4040, a GAL (generic array logic) Type 20V8 and a handful of discrete components to furnish the central clock frequency. The GAL is the central part — here, it forms a kind of junction between a number of clock signals, which are combined into a usable video signal. The design concept of the test pattern generator is illustrated in the block diagram shown in Fig. 1. All synchronization signals are generated digitally, and derived from a single quartz crystal, which ensures accuracy, stability and fixed phase relationships (those of you who have ever tried to design a test pattern generator will confirm the importance of these features). The divide-by-two scaler in the lower left-hand corner of the diagram supplies the PAL chrominance ('colour') subcarrier frequency of 4.433 MHz. It is followed by an XOR gate which supplies a 90° phase-shifted copy of this signal. The section marked as 'PAL switch' determines whether the pulse shaper is fed with the 0° signal or the 90° phase shifted signal. The pulse shaper serves to combine the colour subcarrier with the horizontal and vertical synchronization signals.

The output of the PAL test pattern generator supplies a standard CVBS (chrominance-video-blanking-synchronization, or 'composite video') signal with a level of 1 V into 75 Ω, which corresponds to the load impedance presented by most video recorder and TV video inputs. The second output of the generator supplies TTL-level R, G and B (red, green and blue) signals, along with the combined synchronization pulses. These separate output signals are particularly useful for testing colour monitors.

Colour generation

Generating the colours is the most critical process in the test pattern generator. In a PAL (phase alternating line) encoded video signal, the chrominance ('colour') component, C, is conveyed to the receiver with the aid of a subcarrier at 4.43361875 MHz. This carrier is amplitude-modulated by the colour saturation information, and phase-modulated by the colour information. These two functions rather complicate the design of a good test pattern generator. In particular, due care must be taken to ensure that the subcarrier frequency and the colour burst are sufficiently stable.

In the PAL system, the colour burst is transmitted during the horizontal blanking period (A-H in Fig. 2). It is positioned in the so-called back porch period, and starts 5.6 μs after the falling edge of the line sync pulse. The burst itself consists of 12 periods of the chrominance subcarrier frequency. The phase shift of these periods alternates every other line between 135°

and 225°, which corresponds to a phase shift of 90° (Fig. 3). The phase switching operates at half the line frequency, or 7.8125 kHz. The burst contains two synchronization signals. The average phase shift of 180° serves to synchronize the 4.43 MHz oscillator in the TV set, while the phase changes synchronize the phase switch circuitry contained in the colour decoder.

The line (or 'horizontal') frequency, f_h, and the colour subcarrier frequency, f_c, have a fixed relation:

$$f_c = 283.75\, f_h + 25.$$

Further details on this relation may be found in Ref. 1. In the present generator, this relation is approximately correct by using an offset of 284. This means that the line frequency becomes the quartz frequency divided by two times 284, or

$$f_h = 8.86 \text{ MHz}/568 = 15{,}611 \text{ Hz}.$$

It is necessary to use the factor of two because the crystal used supplies a frequency of two times the desired colour subcarrier frequency (4.43 MHz). This clock frequency of 8.86 MHz makes it much easier to generate a phase shift of 90°. The divide-by-568 function is realized by a counter, IC3 (see the circuit diagram in Fig. 5.). The use of the factor 284 instead of 283.75 has an important advantage during measurements. The fact that the line frequency is coupled to an even number of colour subcarrier periods enables the 'TV line' trigger mode found on many oscilloscopes to be used when viewing the colour burst and related signals in a TV set.

According to the CCIR standard, a PAL television signal has 312.5 lines in every raster. Two rasters are interlaced to form one complete picture or frame. The half line (312.5) allows an easy transition to be made from one raster to another. Interlacing is, however, not generally desirable on test patterns, and is therefore not implemented in the present circuit, which supplies an even number of lines per raster. Based on a line frequency of 15,611 Hz and 312 lines per raster, we obtain a field frequency of 50.036 Hz. The deviation of 0.036 Hz from the standard 50 Hz has no practical significance. The colour signal changes phase (135°/225°) in unison with the burst signal, at a rate equal to half the line frequency. In general, the phase required for the colour is processed during the 135° burst. In terms of the colour signal, this phase shift corresponds to 'orange'. The PAL switch causes this signal to be changed from 135° to 225° by 'mirroring' it against the 0-180° reference (x-axis). Thus, the original 135° (180°−45°) becomes 225° (180°+45°). In the receiver, the new signal phase must be processed in the reverse way to ensure that the original colour is restored. Without this phase reversal, orange and green would appear alternately. The 90° phase reversal on every alternate line is the characteristic difference between the PAL and NTSC (National Television Standards Committee) TV systems. The advantage of PAL over NTSC is that the system is capable of counteracting static phase changes, which would cause colour instability. NTSC does not allow for phase correction, and the acronym is often jocularly said to stand for 'Never The Same Colour'.

If we limit the number of colours supplied by the test pattern generator to two, orange (135°) and green (225°), all that is required are the two 90° phase shifted signals supplied by the previously mentioned 8.86-MHz central clock oscillator. This oscillator is quartz controlled, and has only one transistor. It is a standard design used in many colour TV receivers. Obtaining two 90° phase-shifted clock signals, and halving the central clock frequency is achieved with an XOR gate and a bistable, which are contained in the GAL. The timing of the signals at the input and output of the digital divider and the phase shift circuit is shown in Fig. 4. The operation of the XOR gate is illustrated further in the top right hand corner of the diagram.

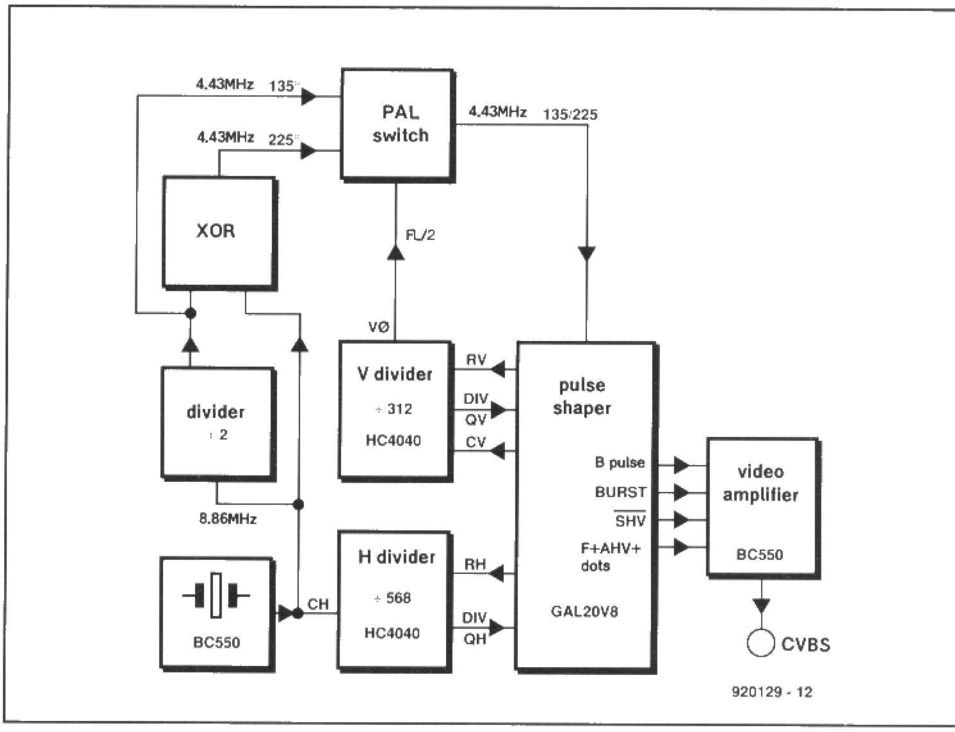


Fig. 1. This block diagram shows the sub-sections of the test pattern generator. Not all blocks are found back in the actual circuit as ICs or active components. This is because most functions indicated here are contained in a GAL (generic array logic) device.

TIMING SPECIFICATION

PAL encoded test signals:
(1). green (225°) or orange (135°).
(2). as (1), but with 4 white vertical bars.

Quartz frequency:	8.88672375 MHz
Colour subcarrier:	4.43361875 MHz
Line frequency:	15,611 Hz (Δ = −14 Hz)
Field frequency:	50.036 Hz (Δ = +0.036 Hz)
Line sync pulse:	4.5 μs (Δ = −0.2 μs)
Front porch:	2.7 μs (Δ = +1.2 μs)
Line blanking:	14.4 μs (Δ = +2.4 μs)
Start of burst:	5.4 μs (Δ = +0.2 μs)
Burst length:	2.7 μs (Δ = +0.45 μs)
Field sync pulse:	0.5 ms (Δ = +0.35 ms)
Field blanking:	1.5 ms (Δ = 0.1 ms)

Deviations (Δ) relative to CCIR recommendation 470 and Report 624.

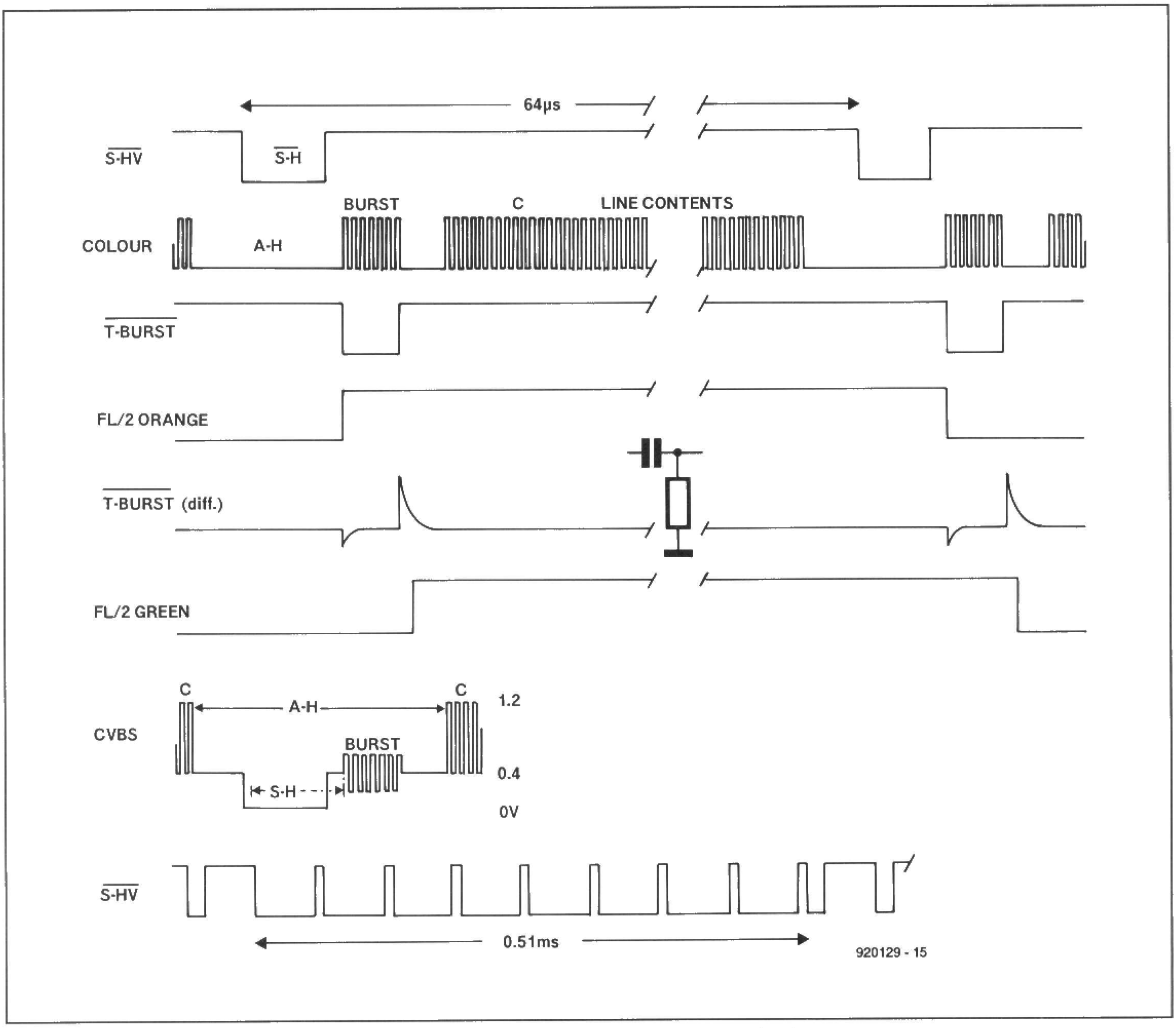


Fig. 2. This timing diagram shows the relation between the most important signals in the circuit.

The burst and the colour signal can have two combinations: either they have the same phase (orange), or they have a phase difference of 90° (green). The selection between these two colours is made with switch S1.

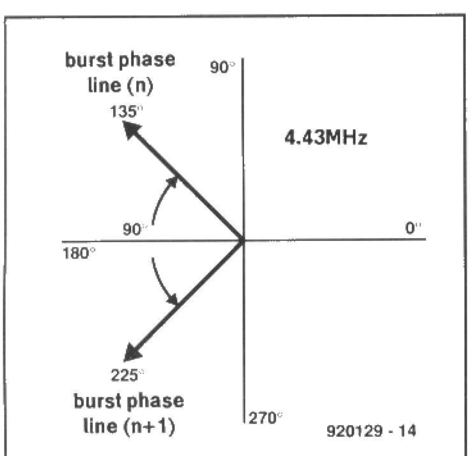


Fig. 3. The phase of the colour burst changes between 135° and 225° every alternate picture line.

The 'vertical' counter, IC2, is clocked with the line frequency, for which the burst pulse (T-burst\) is used. The Q0 output of IC3 supplies the FL/2 signal, i.e., half the line frequency. When T-burst\ is not inverted, the phase is switched before the burst, which results in an orange picture. By contrast, when T-burst\ is differentiated by C2-R2, (Fig. 3, centre), the phase changes a little later, between the burst and the colour signal (Fig. 2). The result is a green test picture.

Inside the GAL

The ready-programmed GAL in the circuit generates a number of digital signals: the inverted burst pulse (T-burst\), the inverted composite synchronization signal (S-HV\) and the composite burst/colour signal (C). These three signals are added in a passive matrix circuit R7-R8-R9-D1, and subsequently buffered by emitter follower T1. Resistors R3 and R4 enable the emitter follower to provide the required source impedance (75 Ω) and signal level (1 V_{pp}). The burst is given the appropriate level and offset by a clipper, R9-D1. These two parts function only when the T-burst signal is active.

The fact that the 4.43 MHz signal is rectangular need not worry us too much. In general, the bandwidth of video amplifiers in video recorders and TV sets is limited to about 8 MHz, so that harmonics of the 4.43-MHz signal do not cause problems.

The line and dot patterns in the test chart have the 4:3 format. There is, however, one flaw in the test pattern: the picture is shifted by 0.3 µs. In

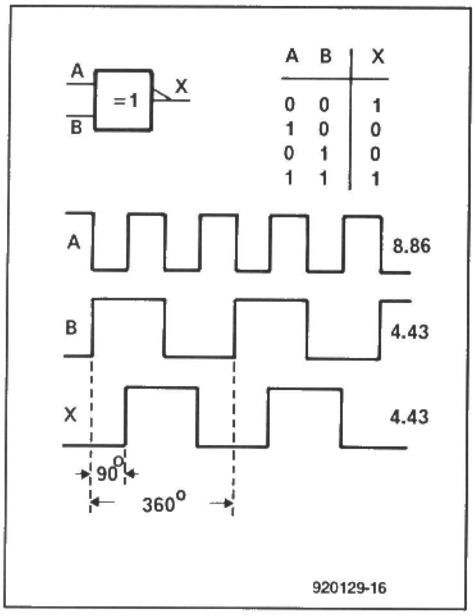
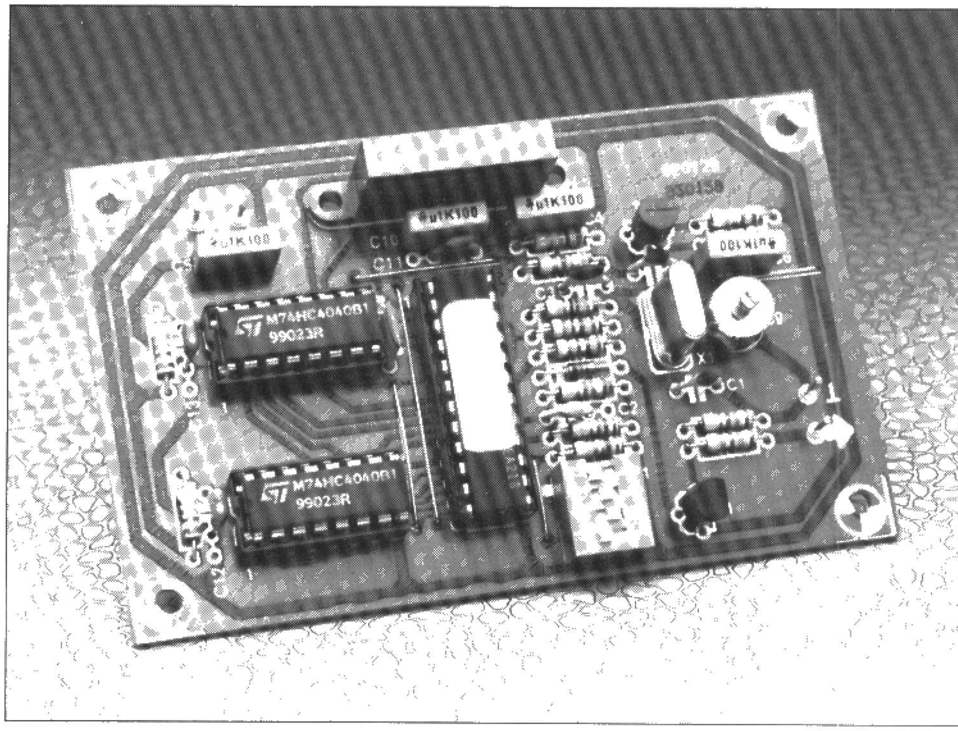


Fig. 4. A bistable (divide-by-two device) and an XOR gate supply two 90° phase shifted signals that are required for the picture generator.



practice, this means that the pattern is not exactly centred on the screen. However, this is not visible from a distance.

Finally, the signals S-HV, R, G and B (Fig. 6) are available with TTL levels on connector K1. These signals also take into account the blanking period, A-H. It should be noted that the signals on K1 are suitable for driving high-impedance inputs only. Buffers such as the HC4049 or the HC4050 are required when low-impedance loads are to be connected — the GAL itself it **not** capable of supplying enough current to drive inputs with an impedance of 75 Ω.

Construction and test

The track layout and component

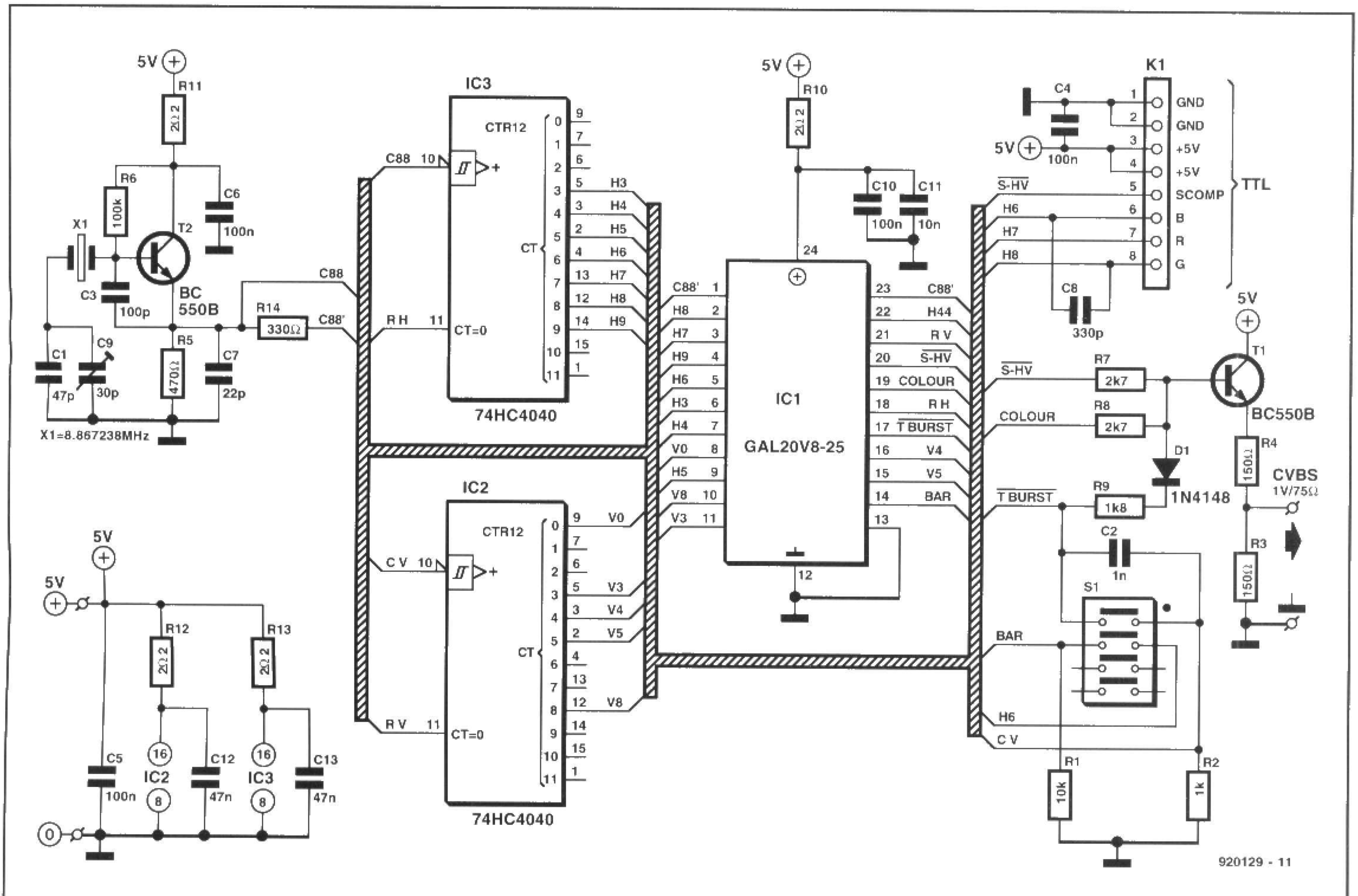


Fig. 5. Circuit diagram of the test pattern generator. Most functions are performed by a single GAL Type 20V8, which is available ready-programmed through our Readers Services.

mounting plan of the printed circuit board designed for the test pattern generator is shown in Fig. 7. Since the circuit operates at relatively high frequencies, construction on, for example, veroboard or stripboard is not recommended. To minimize cross-effects between various sections of the circuit, the dividers (IC2 and IC3) and the GAL (IC1) have individual supply decoupling networks. The *R-C* networks used prevent the ICs from affecting each other's operation via the power supply.

When purchasing components for this project, make sure to use HC types, **not** HCT types, for IC2 and IC3. The DIP switch, S1, may be replaced with two miniature switches which are fitted on the case front panel. The wires between these switches and the board must be kept as short as possible — not longer than a couple of centimetres! The same goes for the wires between the PCB and the output socket.

The adjustment of the circuit is limited to trimmer capacitor C9 in the quartz oscillator. This setting is not critical, and easily carried out with the aid of a properly working TV set. Connect the output of the generator to the CVBS (composite video) input pin

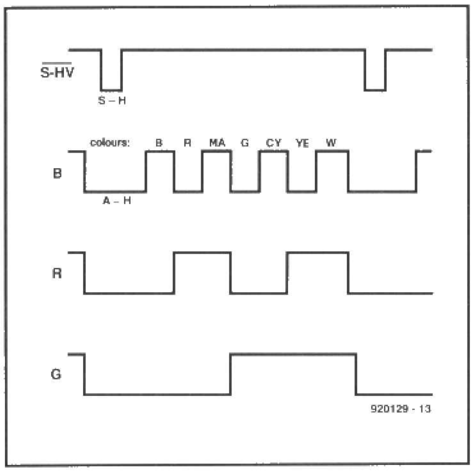


Fig. 6. Timing of the signals at the TTL output (R, G, B and the composite H/V syncs). These signals may be used to put a test pattern with white bars on a colour monitor.

on the SCART plug. Adjust C9 until the colours are stable. The 'lock-and-track' characteristic of the colour decoder inside the TV makes the adjustment of C9 relatively broad. If you are fortunate enough to have access to a frequency meter, connect it to the H44 signal (pin 22 of the GAL), and adjust C9 for a reading of 4.43361857 MHz.

The test pattern generator is not critical in regard of its power supply: all that is needed is a regulated 5-V source capable of supplying an output current of about 60 mA.

The coloured screens supplied by the generator are well suited to checking the operation of sub-circuits in the TV that have to do with the colour processing. In particular, we refer to the colour decoder. The white vertical bars supplied by the generator allow you to check the TV's linearity, focussing and picture position. The bars are selected by the second switch contained in S1. The test pattern then produced is shown in the introductory photograph. ■

Reference:

1. 'Chrominance-locked clock oscillator'. *Elektor Electronics* July/August 1988.

For further reading:

Colour Television (System Principles, Engineering Practice, Applied Technology). By Geoffry Hutson, Peter Shepherd and James Brice. McGraw-Hill, 1990. ISBN 0-07-084199-3.

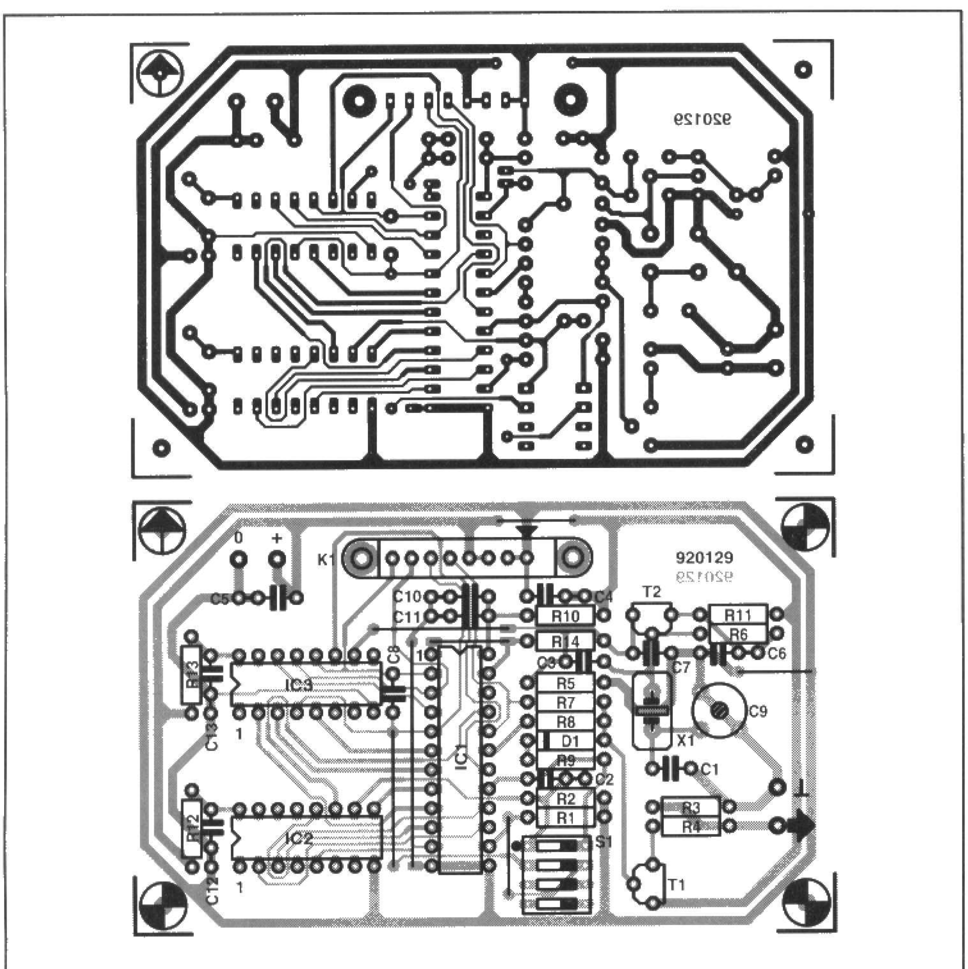


Fig. 7. Track layout (mirror image) and component mounting plan of the printed circuit board designed for the test pattern generator.

COMPONENTS LIST

Resistors:

1	10kΩ	R1
1	1kΩ	R2
2	150Ω	R3;R4
1	470Ω	R5
1	100kΩ	R6
2	2kΩ7	R7;R8
1	1kΩ8	R9
4	2Ω2	R10-R13
1	330Ω	R14

Capacitors:

1	47pF	C1
1	1nF ceramic	C2
1	100pF	C3
4	100nF	C4;C5;C6;C10
1	22pF	C7
1	330pF	C8
1	30pF trimmer	C9
1	10nF ceramic	C11
2	47nF ceramic	C12;C13

Semiconductors:

1	1N4148	D1
2	BC550B	T1;T2
1	GAL20V8-25 (order code ESS6211; see page 70) *	IC1
2	74HC4040	IC2;IC3

Miscellaneous:

1	8-way SIL pin header	K1
1	4-way DIP switch	S1
1	8.867238 MHz quartz crystal	X1
1	Set of printed circuit board and GAL (ready-programmed). Order code: 920129 (see page 70).	

* contained in set 920129

FIGURING IT OUT

PART 1 – INTRODUCING NETWORKS

By Owen Bishop

Here is a new series to help you with the quantitative aspects of electronic design: predicting currents, voltage, waveforms, and other aspects of the behaviour of circuits. Our aim is to provide more than just a collection of rule-of-thumb formulas. We will explain the underlying electronic theory and, whenever appropriate, render some insights into the mathematics involved.

A network consists of two or more impedances joined together by conductors so as to perform a particular function. In the network of Fig. 1 the impedances comprise three resistors, a capacitor, and an inductor, joined in one of the many configurations possible with this particular assortment of components. This network happens to be a complete circuit so it also includes a source of electromotive force (emf, E). But this is not an essential component of a network. The emf may be derived from another connected network.

Figure 1 illustrates the more important terms we use for describing networks:

Elements:the resistors, capacitors and other items joined into the network.

Node (or junction): a point where two or more elements are joined.

Branch: a connection between one node and another, usually containing one or more elements.

Loop: a closed **path** through the network. In Fig. 1, the dashed lines indicate one of the many loops in this network.

Mesh: a loop which does not have any branches linking different parts of it. In Fig. 1, the dotted lines in dicate all 4 meshes of this network.

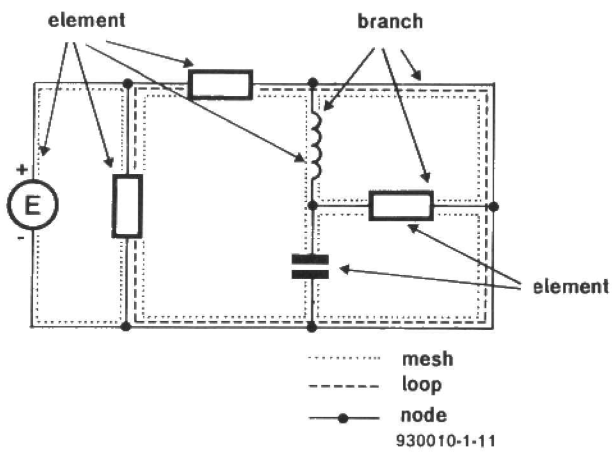


Fig. 1. Terms used to describe a network.

a

b

c

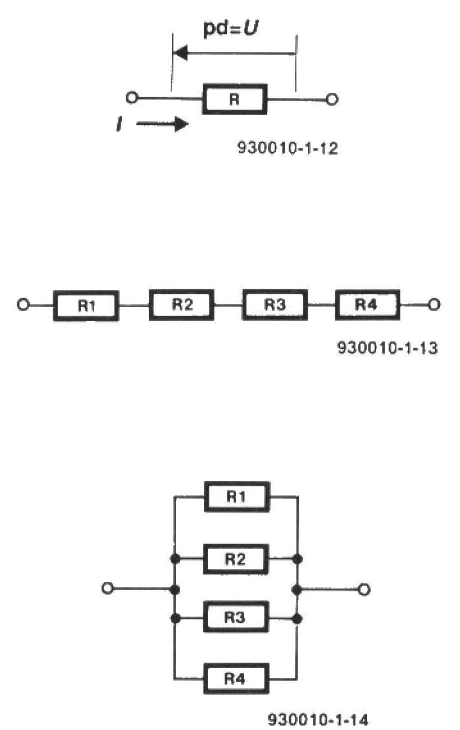


Fig. 2. Illustrating the resistance equations.

Network analysis

The aim of analysing a network is to predict the potential differences (pd) that develop between its nodes and the currents that flow in its branches under the influence of internal or external emfs. Unless it is stated to the contrary, we assume that the conductors themselves have negligible resistance. A consequence of this is that the potential at one end of a conductor is exactly equal to the potential at its other end. We also assume that there are no incidental sources of emf such as might occur by electromagnetic induction from adjacent networks or from thermoelectric effects at the junctions of dissimilar conductors. If any such effects are thought to occur, they must be represented on the network diagram as current or voltage sources of specified magnitude.

We begin the study of analytical techniques by confining our attention to resistive impedance. Resistors are the most usual origin of this; they are deliberately included in the network because they have this property. Resistance may also be exerted by other devices such as inductors, diodes and cells.

The more important equations relevant to resistance are illustrated in Fig. 2.

The definition of the ohm:

$$U/I=R, \qquad \text{[Eq. 1]}$$

where U is the potential difference (in volts, V), I is the current (in amperes, A), and R is the resistance (in ohms, Ω).

Note that the arrow representing the potential difference (pd) across the resistance is directed towards the left. This indicates that the left end of the resistance is at a higher potential (more positive) than the right end. Note, too, that the current is shown flowing from the end at higher potential to the end at lower potential. In almost all instances in this series current

is taken to be conventional current, from positive to negative, **not** electron flow from negative to positive.

Resistances in series:

$R = R_1 + R_2 + R_3 + \ldots$ [Eq. 2]

Resistances in parallel:

$1/R = 1/R_1 + 1/R_2 + 1/R_3 + \ldots$ [Eq. 3]

For two resistances in parallel Eq. 3 simplifies to

$R = R_1R_2/(R_1+R_2)$. [Eq. 4]

Network reduction

If several resistances in a network can be represented by a single resistance, the **equivalent resistance**, subsequent calculations are made much simpler. Reducing the complexity of a network by substituting equivalent resistances wherever possible is an important technique in network analysis.

As an example, take the network of Fig. 3a. The aim is to find a single resistor which, connected between terminals A and B, has a resistance equivalent to that of the three resistors shown. The problem is solved in stages. The first stage is to replace the 4 Ω and 2 Ω resistors by a single equivalent resistor, R_{CD}. Equation 2 gives

$R_{CD} = 4+2 = 6$ Ω.

The equivalent network in Fig. 3b at this stage has two 6 Ω resistors in parallel. Equation 4 gives

$R_{AB} = 6 \times 6/(6+6) = 3$ Ω.

Figure 3c shows the final result: the equivalent resistance is 3Ω. For a range of p.d.s. applied across A and B, the corresponding currents flowing from A to B are unaffected by whether the network consists of the three original resistors or is replaced by a single 3 Ω resistor.

Another example is shown in Fig. 4a. R_{DE} is the equivalent of 10 Ω and 30 Ω in parallel (Eq. 4):

$R_{DE} = 10 \times 30/(10+30) = 7.5$ Ω.

This gives Fig. 4b. The equivalent resistance of this is 20 Ω, 30 Ω and 7.5 Ω in series; by Eq. 2:

$R_{AB} = 20+30+7.5 = 57.5$ Ω.

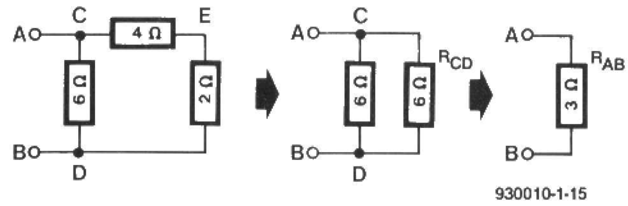


Fig. 3. Network reduction.

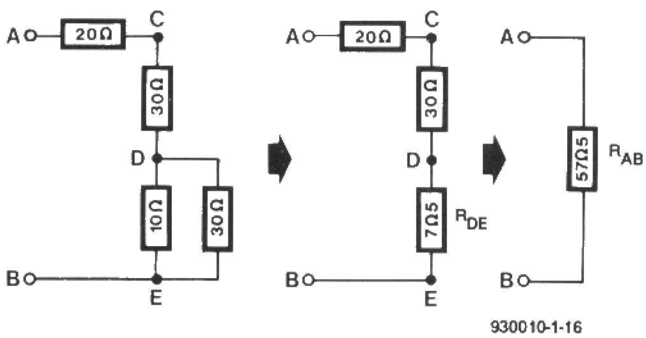


Fig. 4. Network reduction – another example.

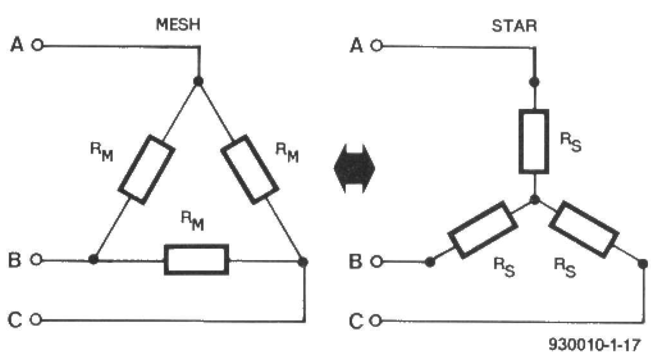


Fig. 5. Mesh–star transformation with equal resistances.

Mesh–star transformation

In some networks it is useful to be able to replace one configuration of resistors with another **configuration** that has the same resistive properties. A commonly used tactic is to replace the mesh connection by the equivalent star connection in Fig. 5. Both networks have three terminals and we have to replace Fig. 5a with Fig. 5b while retaining the same resistances between each pair of terminals.

First of all consider the simplest case where all three resistors of Fig. 5a have equal value, R_M, and are to be replaced by three resistors of equal value R_S. Using the same equations as in the previous paragraph, we find the equivalent resistance between any pair of terminals, say, between A and B. Redrawing the mesh diagram, while keeping the connections the same, we can see in Fig. 6 that there are two resistors of value R_M in series. Their equivalent resistance is $2R_M$. This pair is in parallel with a single resistor and equation 4 gives:

$$R_{AB} = R_M \times 2R_M/(R_M+R_M) =$$

$$= 2R_M^2/3R_M = 2R_M/3. \text{ [Eq. 5]}$$

In the star configuration, the resistor connected to terminal C may be ignored when we are considering the resistance between A and B. There are just two resistors in series between A and B:

$R_{AB} = 2R_S$. [Eq. 6]

If Fig. 5b is to be a replacement for Fig. 5a, the value of

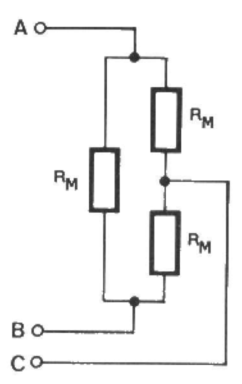


Fig. 6. Redrawn version of Fig. 5a.

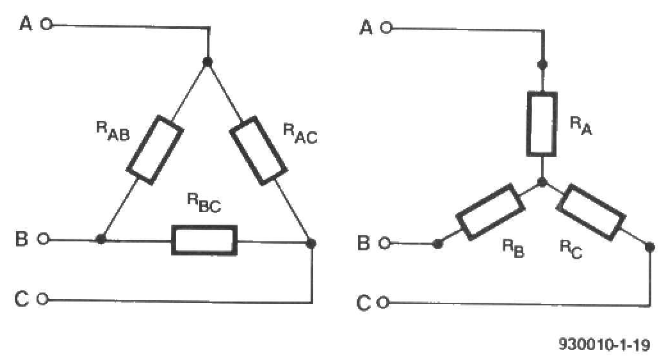


Fig. 7. Mesh–star transformation with unequal resistances.

R_{AB} must be the same in both. Combining equations 5 and 6:

$2R_M/3=2R_S$, so that $R_M=3R_S$.

Since the networks are symmetrical, the same result is obtained when we take pairs of terminals A and C or B and C. Summing up, if the three resistors are reduced to one third their original value, the mesh of Fig. 5a may be replaced by the star of Fig. 5b. Conversely, a star network can be replaced by a mesh network in which the resistors have three times their original value.

If the networks consist of resistors of **unequal** value, the calculations become rather more involved, though the principle of using equations 2 and 4 remains the same. It is left to the reader to show that, in Fig. 7:

$R_A=R_{AB}\times R_{AC}/(R_{AB}+R_{AC}+R_{BC})$.

The rule for R_A is to multiply together the two resistances connected to terminal A, then divide by the sum of all three resistances; R_B and R_C are calculated in a similar way.

The reverse transformation, from star to mesh, uses equations of the form:

$R_{AB}=R_A+R_B+R_AR_B/R_C$.

Note that the mesh network is sometimes referred to as the delta, or Δ, network, and the star network as the wye, or Y, network.

When we are given a network to analyse, the calculations may often be shortened by substituting a star network for a mesh network, or the other way about. In this example, we use the mesh–star transformation to analyse Fig. 8a. The three 12 Ω resistors are not drawn in a triangle, but it is easy to see that this is really a mesh network with three equal resistances. In Fig. 8b this is replaced by the corresponding star network with resistors of one third the value. Replacing the resistors that are in series, the network reduces to Fig. 8c. The 12 Ω and 8 Ω resistances are equivalent to

$12\times8/(12+8)=3.6\ \Omega$,

which, in series with 4 Ω, gives 7.6 Ω as the equivalent resistance for the whole network.

We consider the network of Fig. 9a as a star network of three 6 Ω resistors in parallel with a

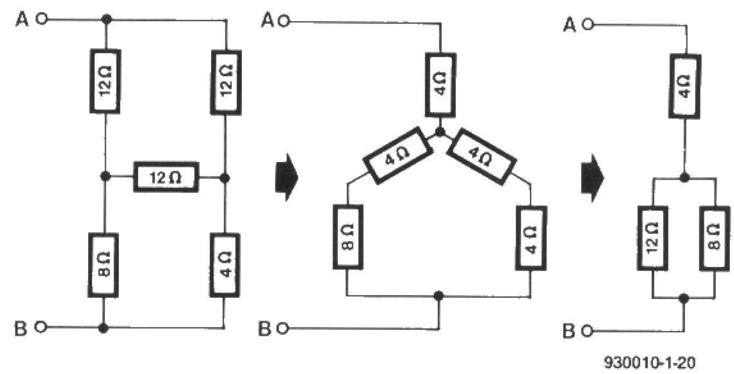


Fig. 8. Using the mesh–star transformation.

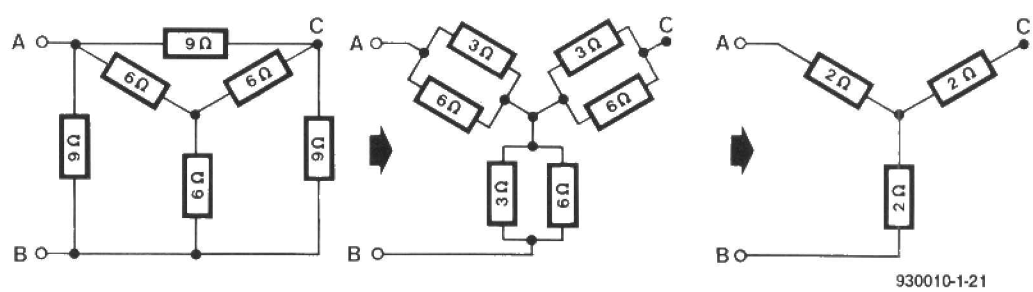


Fig. 9. Another example of the mesh–star transformation.

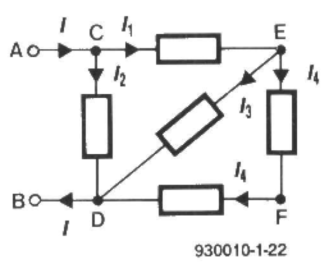


Fig. 10. Kirchhoff's Current Law.

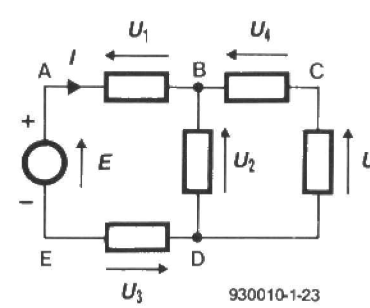


Fig. 11. Kirchhoff's Voltage Law.

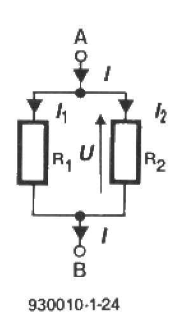


Fig. 12. Current division.

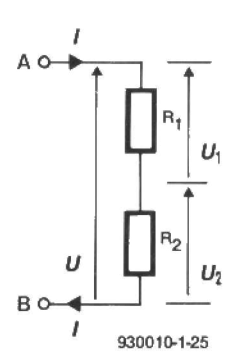


Fig. 13. Potential division.

mesh network of three 9 Ω resistors. Replace the mesh with a star of 3 Ω (one third of 9 Ω) resistors as in Fig. 9b. This reduces to a star of 2 Ω resistors—see Fig. 9c. In calculating the resistance from A to B, we can ignore the arm of the star leading to C, so the equivalent resistance of the whole network is 4 Ω.

Both of the examples given are based on networks with resistors of equal values, but the same principle applies if resistors are unequal.

Kirchhoff's laws

These two laws have many applications in network analysis.

Kirchhoff's current law, known for short as KCL, states that the sum of the branch currents at a node is zero ($\Sigma I=0$). Put another way, it states that the total current flowing into a node equals the total current flowing out of it. If currents are varying, KCL applies for every instant of time.

In Fig. 10, the currents are given arbitrary directions; a current that is actually flowing in the opposite direction to its arrow is regarded as a negative current. The current flowing out of the network must be equal to that flowing into it, so we show current I flowing in at A and out at B.

For the nodes in this figure, KCL gives the following equalities:

node C: $I-I_1-I_2=0$;

node D: $I_2+I_3+I_4-I=0$; node E: $I_1-I_3-I_4=0$.

If the values of some of these currents are known, it is possible to calculate some of the others.

Kirchhoff's voltage law, or KVL, states that the sum of the branch voltages around a loop is zero ($\Sigma U=0$). In any branch of a network, there is a potential difference (pd) across the element. This may be the direct result of the element being a source of emf, or may be produced when a current flows through a resistive element. The arrows in Fig. 11 indicate the polarity of each pd, pointing from low to high potential. If we travel round a loop in one particular direction (conventionally, clockwise), these pds may be taken as rises or falls of potential. By KVL, the total of the rises **minus** the total of the falls is zero for any loop in the network.

Travelling around the loop ABDE in Fig. 11 in the same direction as the current, there are three falls of potential: U_1, U_2 and U_3. As we pass through the voltage source in the same direction as the current, there is a rise in potential, E. By KVL, from A back to A:

$$E-(U_1+U_2+U_3)=0.$$

By KVL, from B back to B:

$$U_2-(U_4+U_5)=0.$$

We shall cite KCL and KVL frequently in future discussions of circuit behaviour. Below are two simple examples of their application.

Current division

It follows from KCL that, when a current arrives at a point where two or more resistances are connected in parallel—see Fig. 12—it divides into two or more currents. The **total** current remains unchanged. For the two resistors, Eq. 1 gives:

$$U=I_1R_1, \qquad \text{[Eq. 7]}$$

and

$$U=I_2R_2. \qquad \text{[Eq. 8]}$$

Equating the right-hand sides of Eq. 7 and Eq. 8 gives:

$$I_1R_1=I_2R_2,$$

$$\therefore\ I_1/I_2=R_2/R_1. \qquad \text{[Eq. 9]}$$

That is, the currents are **inversely** proportional to the resistances.

As an example, suppose that I=6 A, R_1=4 Ω and R_2=8 Ω. Then, by Eq. 9:

$$I_1/I_2=8/4=2,$$

$$\therefore\ I_1=2I_2. \qquad \text{[Eq. 10]}$$

But we are given that I=6 A, so, by KCL:

$$I=I_1+I_2=6. \qquad \text{[Eq. 11]}$$

From Eq. 10 and Eq. 11, we find that I_1=4 A and I_2=2 A.

Potential division

It follows from KVL that, if two or more resistances in series have a pd across them, the sum of the pds across them equals the total pd across the whole chain—see Fig. 13. The same current I flows through each resistance (KCL). Given a chain of two resistors:

$$I=U_1/R_1=U_2/R_2,$$

$$\therefore\ U_1/U_2=R_1/R_2.$$

That is, the pds are **directly** proportional to the resistances. For example, if U=10 V, R_1=2 Ω and R_2=3 Ω,

$$U_1/U_2=2/3,$$

$$\therefore\ U_1=2U_2/3. \qquad \text{[Eq. 12]}$$

By KVL,

$$U=U_1+U_2=10. \qquad \text{[Eq. 13]}$$

From Eq. 12 and Eq. 13 we find that U_1=4 V and U_2=6 V. Potential dividing networks of this kind are in frequent use in circuits. ■

Next month: more applications of KCL and KVL, and two powerful theorems which aid network analysis.

Test yourself

1. Find the equivalent resistance of each of the five networks of Fig. 14.
2. Analyse Fig. 9a by considering it as two **mesh** networks in parallel, and show that the result is the same as obtained previously.
3. In Fig. 14e, given that I=2 A, calculate I_1 and I_2. Then calculate the pds across AB and each of the resistors.

Answers will be given in next month's instalment.

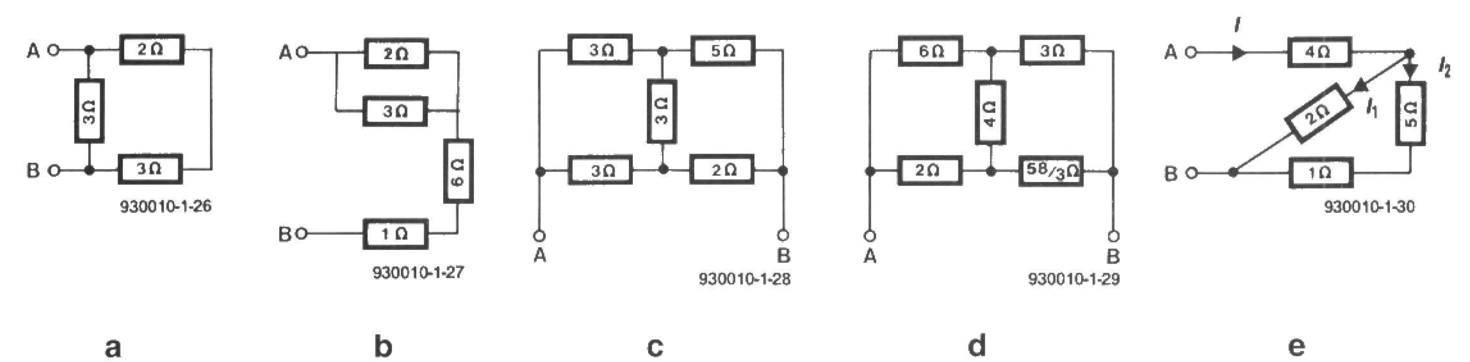


Fig. 14. Networks for TEST YOURSELF.

MULTICORE CABLE TESTER

Design by B.C. Zschocke

Although installing a long multicore cable, or testing such a cable, is facilitated by the colour coding of the individual wires, it still needs two people to carry out the job. Even then, work proceeds satisfactorily and speedily only if these people are within earshot of each other. The tester described in this article overcomes these difficulties; it enables one person to do the work, who can identify each wire unmistakably and locate short-circuits and open circuits

The principle of the design is shown in Fig. 2. The master unit contains a current source that is switched on and off by a rectangular voltage. The current is taken via two wires to the slave unit, where the wires are terminated into resistor R_8. The rectangular voltage across the resistor triggers delay circuit τ, which after a short interval, but still during the pulse, closes a switch. This results in the voltage briefly dipping, which is identified by the master unit as a logic 1. When the two wires are interchanged at the master unit, there will still be a rectangular voltage across R_8, but this will not trigger the delay circuit—the master unit will then register a logic 0.

It will be clear that the tester depends entirely on the current pulses generated by the master unit. In other words, the master unit outputs current pulses and the slave unit receives them

Each current pulse causes one long voltage pulse, or two short ones, across R_8, that is, across the input of the slave unit and, consequently, across the output terminals of the master unit. In other words, the slave unit outputs voltage pulses and the master unit receives them.

So far, so good as far as two wires are concerned. To perform the function over more than two wires, the master unit generates not one pulse but a train of eight pulses. The resulting 8-bit number enables up to 255 wires to be identified (0 means no connection) if the number is binary coded, or 99 wires if a BCD (binary coded decimal) code is used.

How the eight bits are formed into a pulse train is described with reference to Fig. 2, starting with the power supply for the slave unit. This is derived from the pulses provided by the master unit. This saves energy, because the slave unit is on only when required. The pulses are applied to the slave unit via a multiphase bridge rectifier, which makes it immaterial to which two of the many inputs of the slave unit (=wires contained in cable) the master is connected. The pulse is thus applied to the 'timing' block and to the + input of the power supply. The earths of the master and slave unit are interlinked at the same time. A regulator and buffer capacitor ensure continuity of the power supply during the pauses between successive pulses.

The pulses arrive at the timing circuit in trains of eight, followed by a pause of the same length as the eight pulses. During the pause, the timing circuit checks whether the shift register needs to be reset. Also, it arranges for a logic 1 to be clocked into the shift register at the first of the eight

Technical data

Master unit

2-figure display of the wire number (1–99)

Separate earth lead not required

Identifies short-circuits and open circuits

Suitable for long cables

Supply requirements: 9 V battery

Can be extended (DIY!) for use with 1–255 wires

Slave unit

Supply requirements: derived from master unit

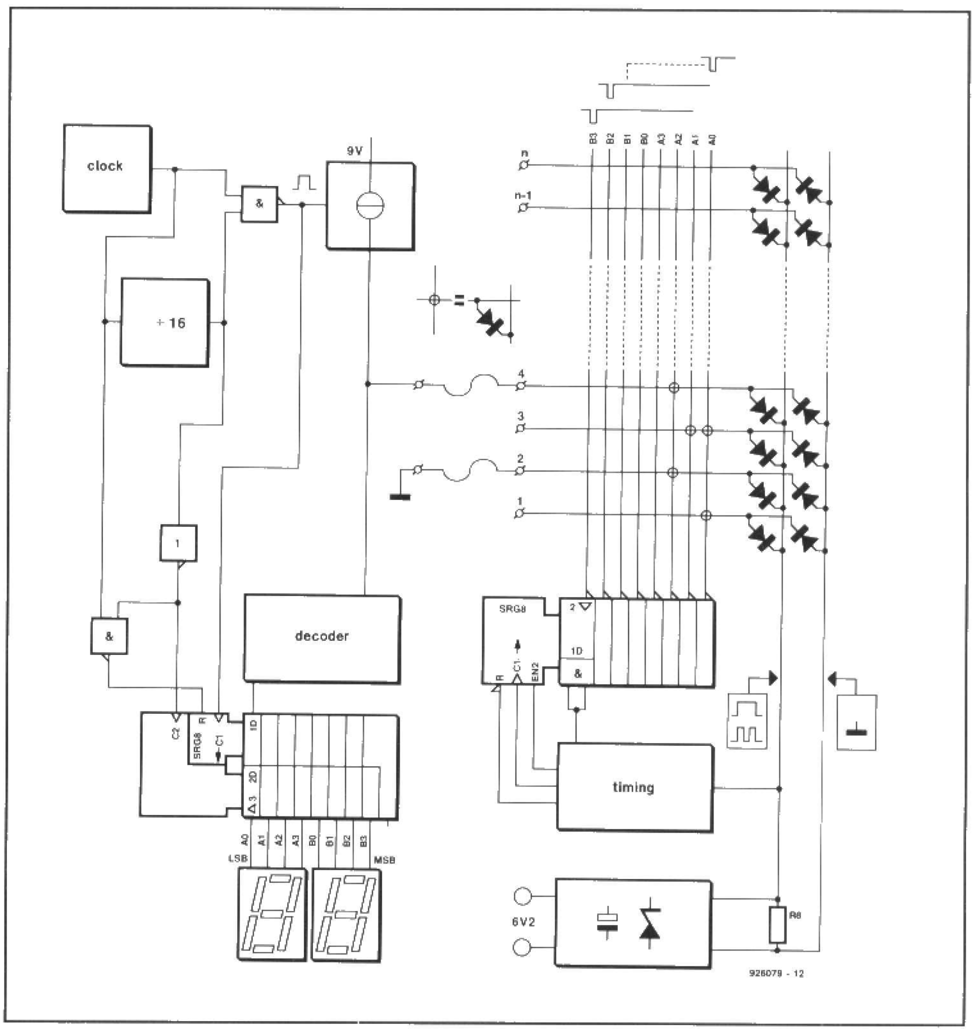


Fig. 1. Block diagram of the multicore cable tester.

pulses. This 1 is shifted by one position for each successive pulse.

Moreover, the timing circuit, in conjunction with the enable input of the shift register, ensures that this single 1 pulls down one of the columns of the diode matrix, A0–B3, at exactly the centre of the pulse.

The placing, or omitting, of diodes in the diode matrix determines whether a pulse in the train is translated in the slave unit into a 1 or not. Allocating a different code to each of the matrix columns gives each connection, and thus each wire, its own unique number.

A break in a wire is identified by the master output remaining logic 0.

A short-circuit is indicated by the display showing a number that cannot be true or strange symbols. It may also happen that an unexpected number is shown and repeated, while the correct number cannot be found.

The clock that drives the system consists of a generator, a ÷16 divider and a NAND gate. This arrangement results in a train of eight pulses, followed by a pause of eight clock periods. This signal is used to control the shift register and the current source mentioned earlier.

During each pulse provided by the current source, the decoder determines from the potential between the two connected wires whether the slave has generated a 1 or a 0. The decoded bit is then input into the shift register at the end of the pulse. When all pulses have been input, they are clocked into the parallel output register of the shift register, whereupon the shift register is reset.

The bits are then taken from the output register to the display that translates them into a legible number. Numbers 00–99 may be displayed if the diode matrix is programmed in BCD code (more about this later). In this arrangement two standard BCD-to-seven-segment decoders suffice to drive the displays. A binary-coded matrix requires three binary-to-seven-segment decoders, which, in discrete designs, need a fair amount of space (PALs are not necessarily a solution here). So as to keep the units small, the present design uses BCD code. The PCB for the master unit has a connector, however, to which a DIY designed decoder may be connected (more about this in the circuit description).

The master unit

In Fig. 3, LD_1 is the least significant digit of the display. Resistors R_1–R_{14} provide current limiting for the display segments, while IC_1 and IC_2 are the BCD decoders. These circuits are controlled by the parallel register in shift register, IC_3. The eight outputs of the register are accessible from outside via K_1 to enable the use of a decoder to drive a hexadecimal or 3-digit BCD display if 255 wires are to be connected.

The clock generator, IC_4, is a Type 4060. Schmitt trigger IC_5 and network R_{15}-C_5 ensure that the transition (edge) at which data are clocked into the shift register is delayed by a very short time relative to the transition at which the previous bit was shifted into the register.

The decoder is formed by IC_{6a} and IC_{6b}. Data are provided via IC_{5c}. Circuit IC_{6b} delays the pulse train by $^1/_{64}$ of a period, so that at each current pulse IC_{6a} is reset. Immediately after the onset of the pulse, the set input is enabled. If the voltage from the slave unit has a dip, IC_{6a} is clocked, the data input is low and the inverting output goes high (a 1 has been decoded!). If the voltage does not have a dip, the bistable remains set and the inverting output stays low.

The necessary signal is generated by current source T_1, which is controlled by the clock via T_2. The current results in a voltage in the slave unit that may be as high as 9 V, that is, U^+. Since this

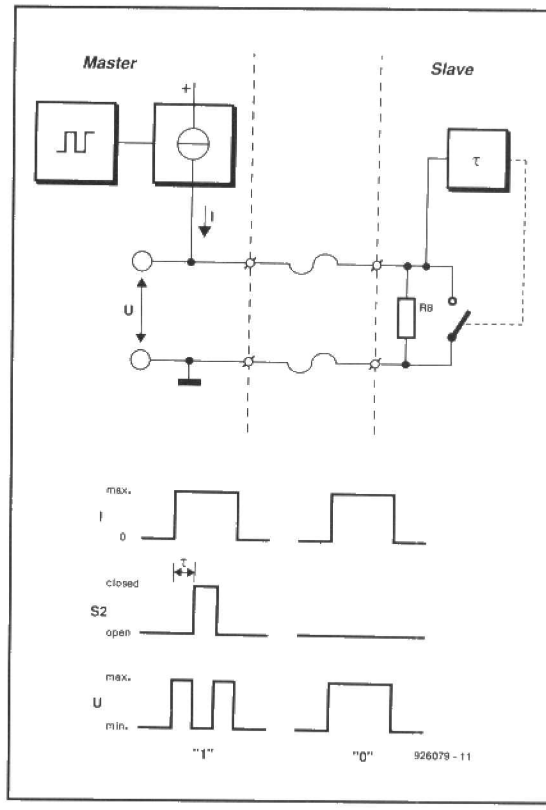


Fig. 2. The principle of the tester.

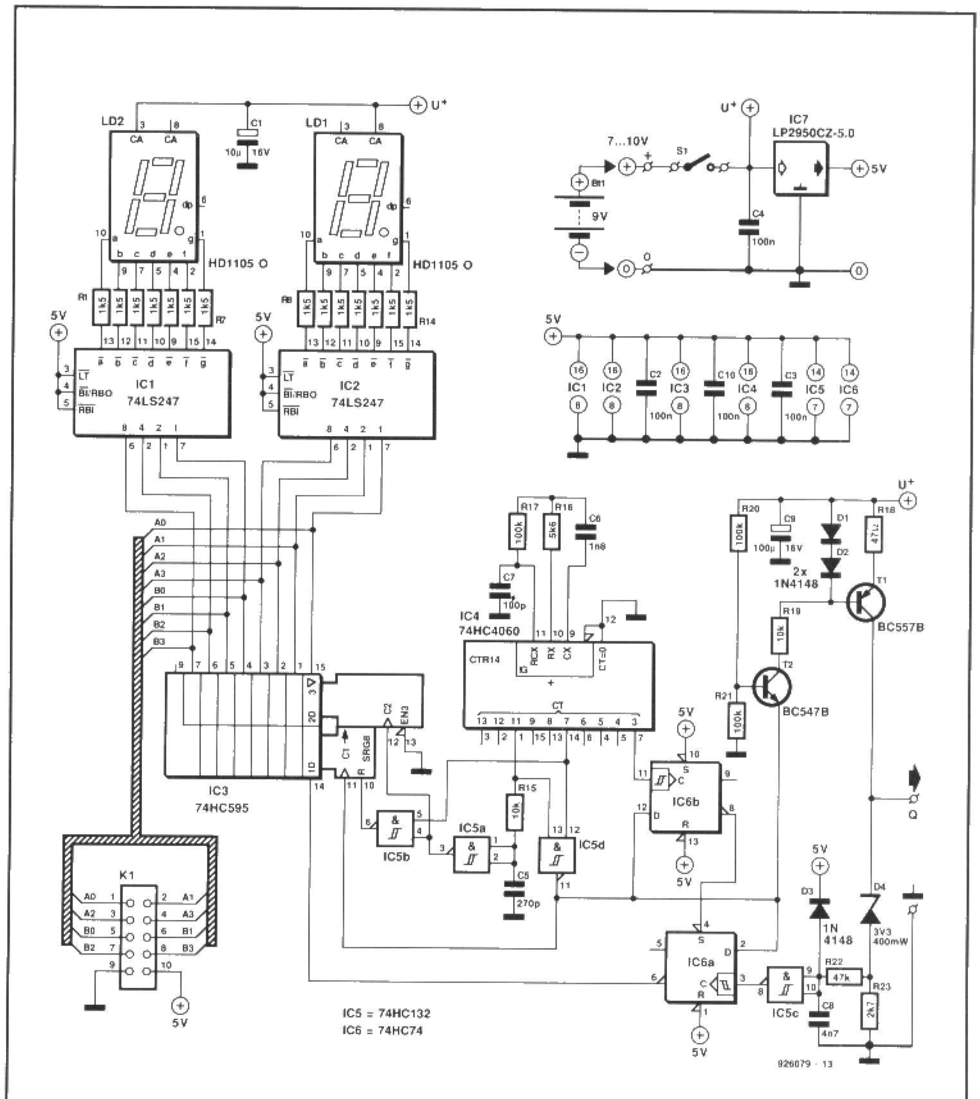


Fig. 3. Circuit diagram of the master unit.

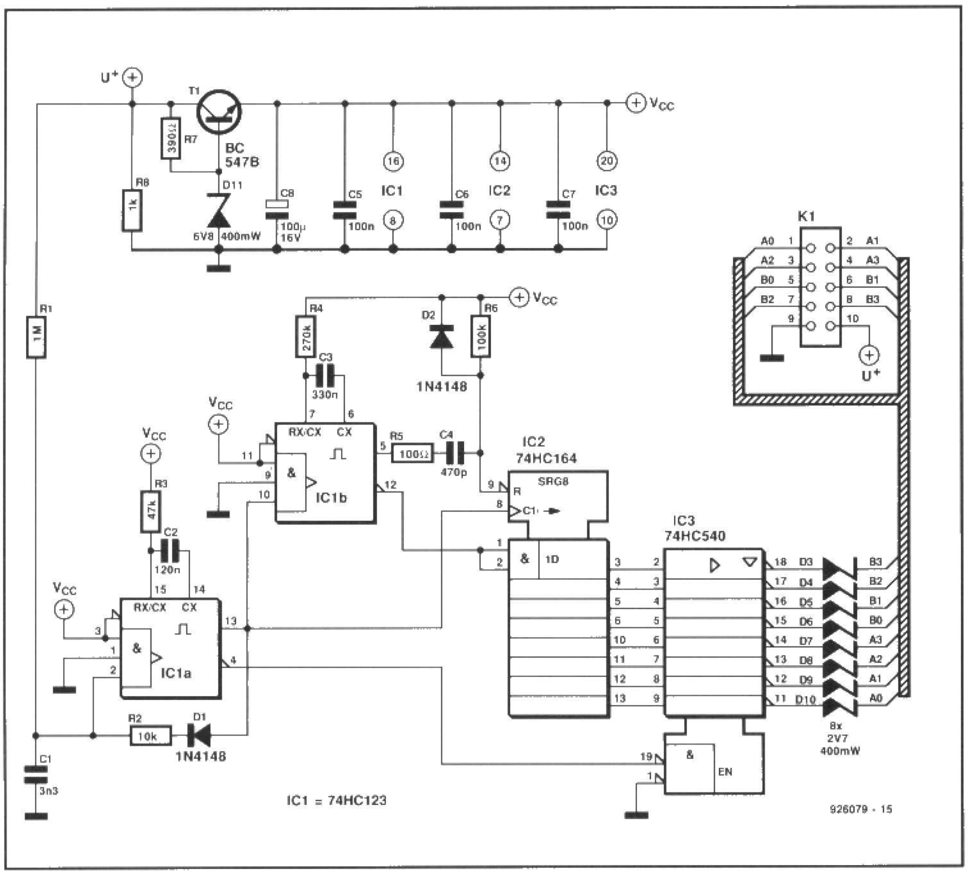


Fig.4. Circuit diagram of the slave unit.

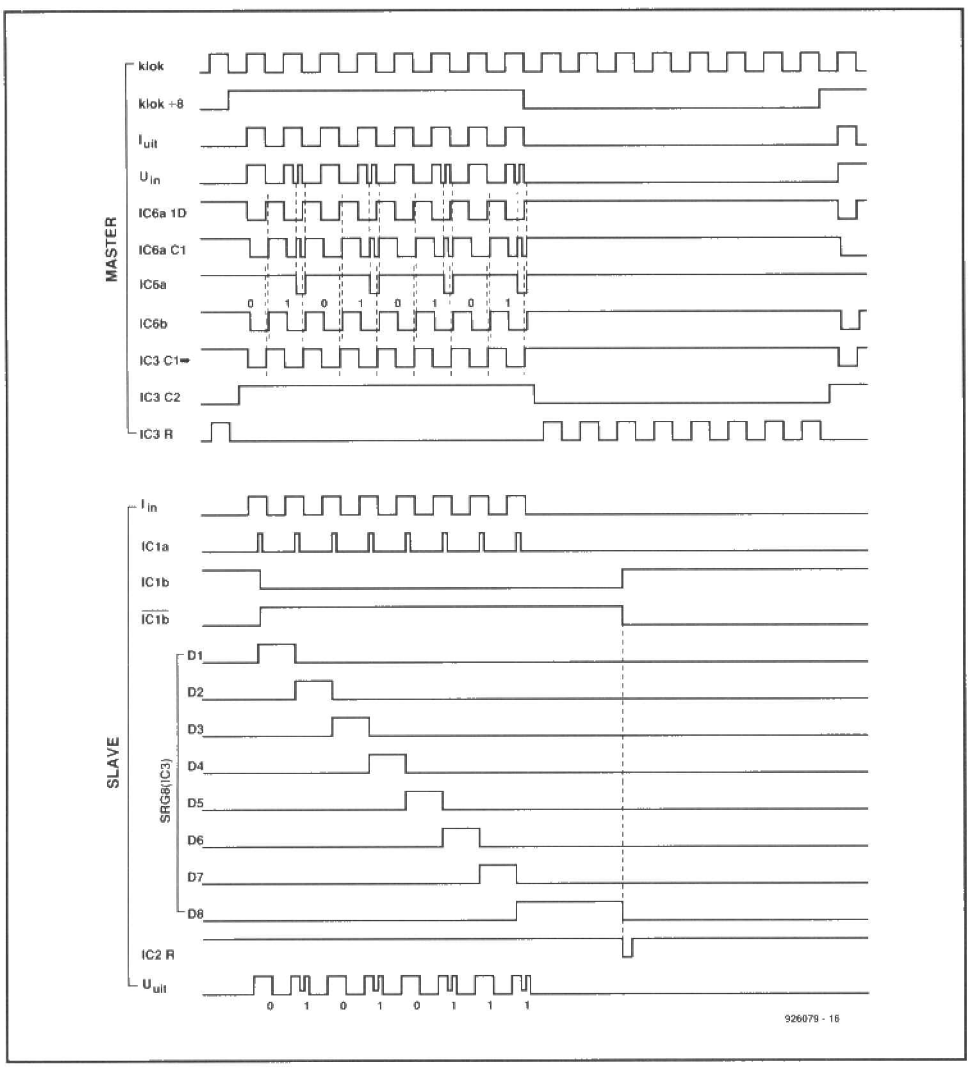


Fig. 5. Timing diagram.

is too high for the decoder, it is lowered by D_4 by 3.3 V. Any residual voltage peaks are smoothed by D_3. Since the dip in the voltage from the slave unit does not drop below 3.3 V (as will be explained later), D_4 also ensures that the decoder identifies the dip as a 0 (3.3–3.3=0). A timing diagram for the master and the slave unit is given in Fig. 5.

The power supply for the tester is provided by six C/R14/HP11 batteries, from which a current of up to 100 mA is drawn (reason for not using a 9 V battery). Remember also that these batteries supply the slave unit.

The battery voltage is used directly for the seven-segment displays and the current source and regulated, by IC_7, for the remainder of the circuitry. The reg-

PARTS LIST

Master unit

Resistors:
R1–R4 = 1.5 kΩ
R15, R19 = 10 kΩ
R16 = 5.6 kΩ
R17, R20, R21 = 100 kΩ
R18 = 47 Ω
R22 = 47 kΩ
R23 = 2.7 kΩ

Capacitors:
C1 = 10 µF, 16 V
C2–C4, C10 = 100 nF
C5 = 270 pF
C6 = 1.8 nF
C7 = 100 pF
C8 = 4.7 nF
C9 = 100 µF, 16 V

Semiconductors:
D1–D3 = 1N4148
D4 = zener 3.3 V, 400 mW
LD1, LD2 = HD1105-0
T1 = BC557B
T2 = BC547B
IC1, IC2 = 74LS247
IC3 = 74HC595
IC4 = 74HC4060
IC5 = 74HC132
IC6 = 74HC74
IC7 = LP2950CZ-5.0 (National Semiconductor)

Miscellaneous:
Bt1–Bt6 = C/R14/HP11 battery
K1 = 10-way flatcable copnnector for PCB mounting
S1 = miniature switch
banana socket (red)
banana plug (black)
Enclosure 125×49×70 mm (eg.,Retex Type RG2)
PCB Type 926085

Matrix board

Semiconductors:
D1–D200 = 1N4148 (max. 119)

→

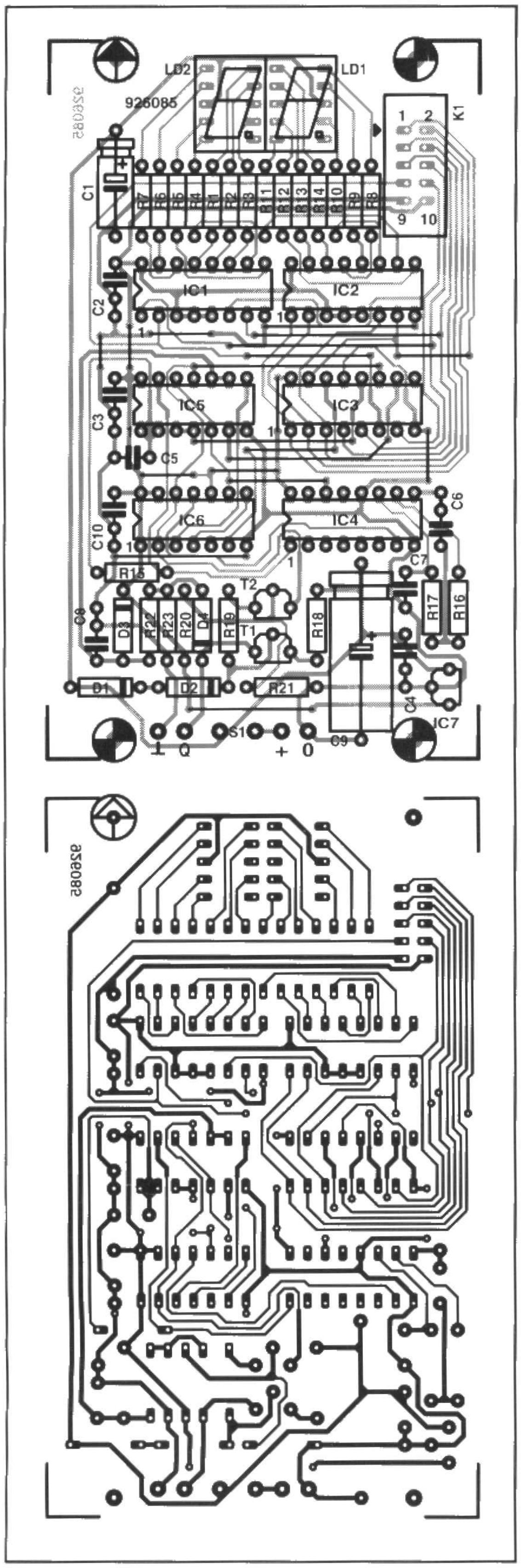


Fig. 6. Printed-circuit board for the master unit.

Miscellaneous:
K1, K2 = 10-way flatcable connector for PCB mounting
20 mini (1 mm) banana sockets for PCB mounting
PCB Type 926079)

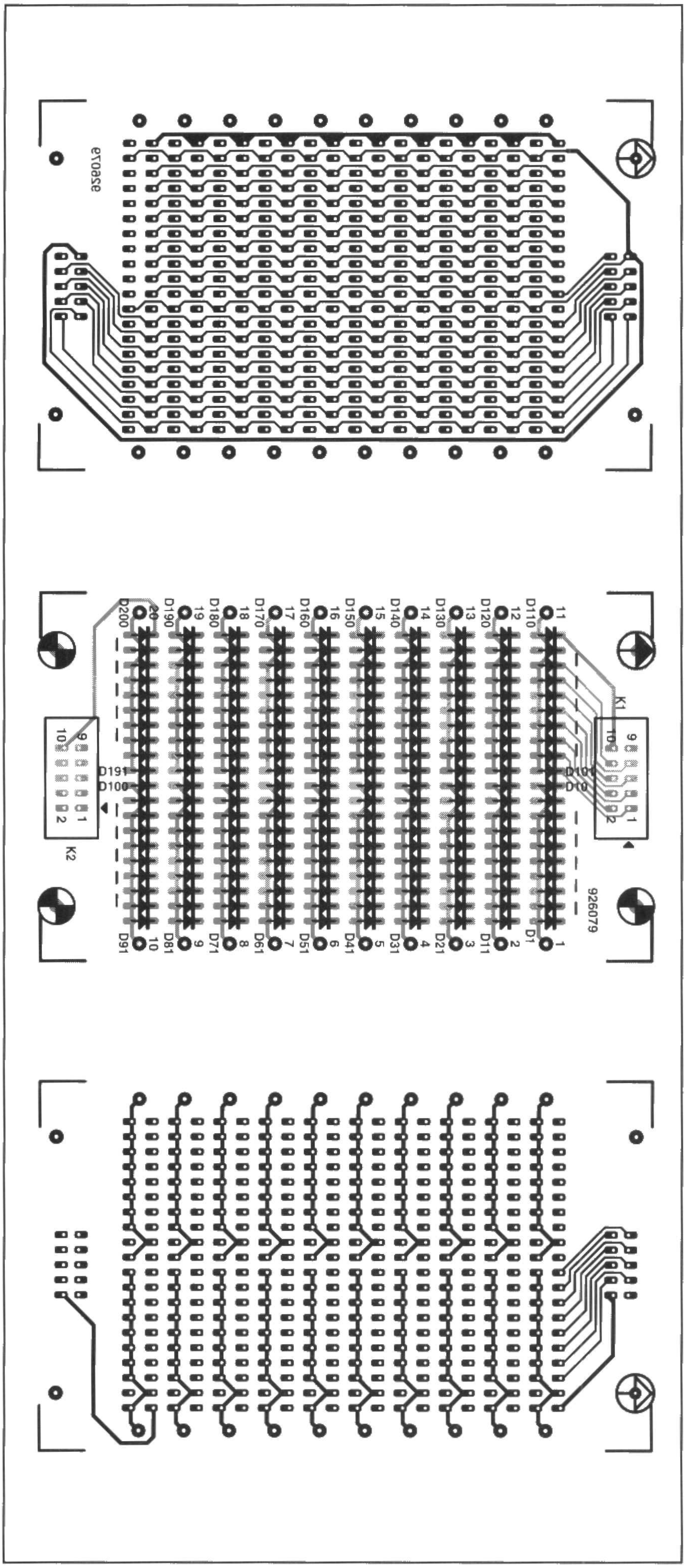


Fig. 7. Printed-circuit board for the diode matrix.

ulator used has low dissipation and requires an input voltage of only 5.4 V.

The matrix

The diode matrix is the largest and most important part of the slave unit. The rectifier bridge in it ensures that the incoming signal from the master unit is always connected to the correct location, irrespective of on which two wires the signal arrives. The signal is first of all applied to the earth line and the U^+ line via the diodes whose circuit designation ends in a 9 or 0 respectively. The remaining diodes form the matrix proper which determines what code the slave unit gives to the connected wires. Since the board has room for connecting 20 wires only, five boards are cascaded via K_1 and K_2.

Setting the codes is straightforward. All diodes, other than those whose designation ends in 0 or 9, correspond to the eight bits of the code, that is, diodes with a designation that ends in 1 represent the least significant bit (LSB) and those with a designation that ends in 8 represent the most significant bit (MSB). Locations where a diode is used correspond to a logic 1 (high), and those where no diode is used to a logic 0 (low). Since a BCD code is used, the first four bits form the least significant number and the other four the most significant number. The whole arrangement is summarized in Table 1.

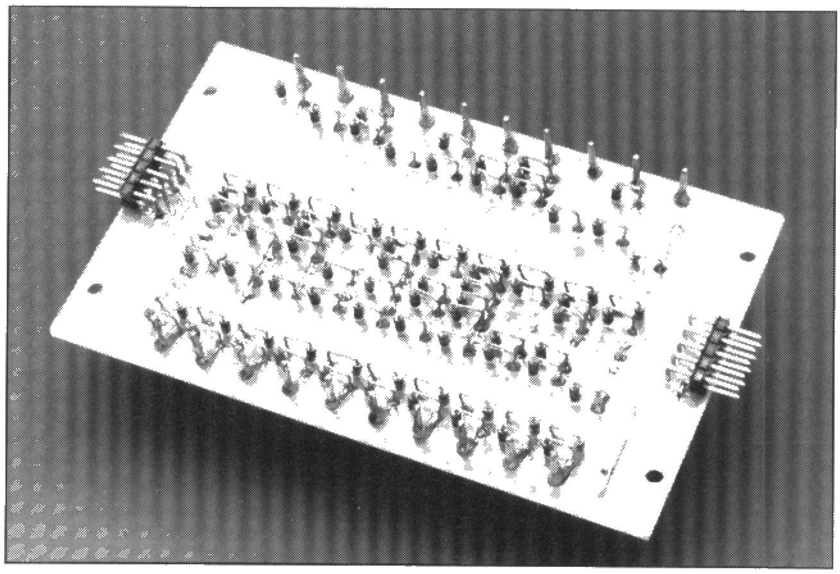
Since logic 0s do not require a diode, the matrix board never needs more than 119 diodes. The exact number depends on the number of wires—see Table 2.

	D..4 A3	D..3 A2	D..2 A1	D..1 A0
	D..8 B3	D..7 B2	D..6 B1	D..5 B0
0	×	×	×	×
1	×	×	×	–
2	×	×	–	×
3	×	×	–	–
4	×	–	×	×
5	×	–	×	–
6	×	–	–	×
7	×	–	–	–
8	–	×	×	×
9	–	×	×	–

Table 1. BCD coding of diode matrix.

Output	Number of diodes
1–20	81
21–40	100
41–60	101
61–80	119
81–99	99

Table 2. Number of diodes per matrix.



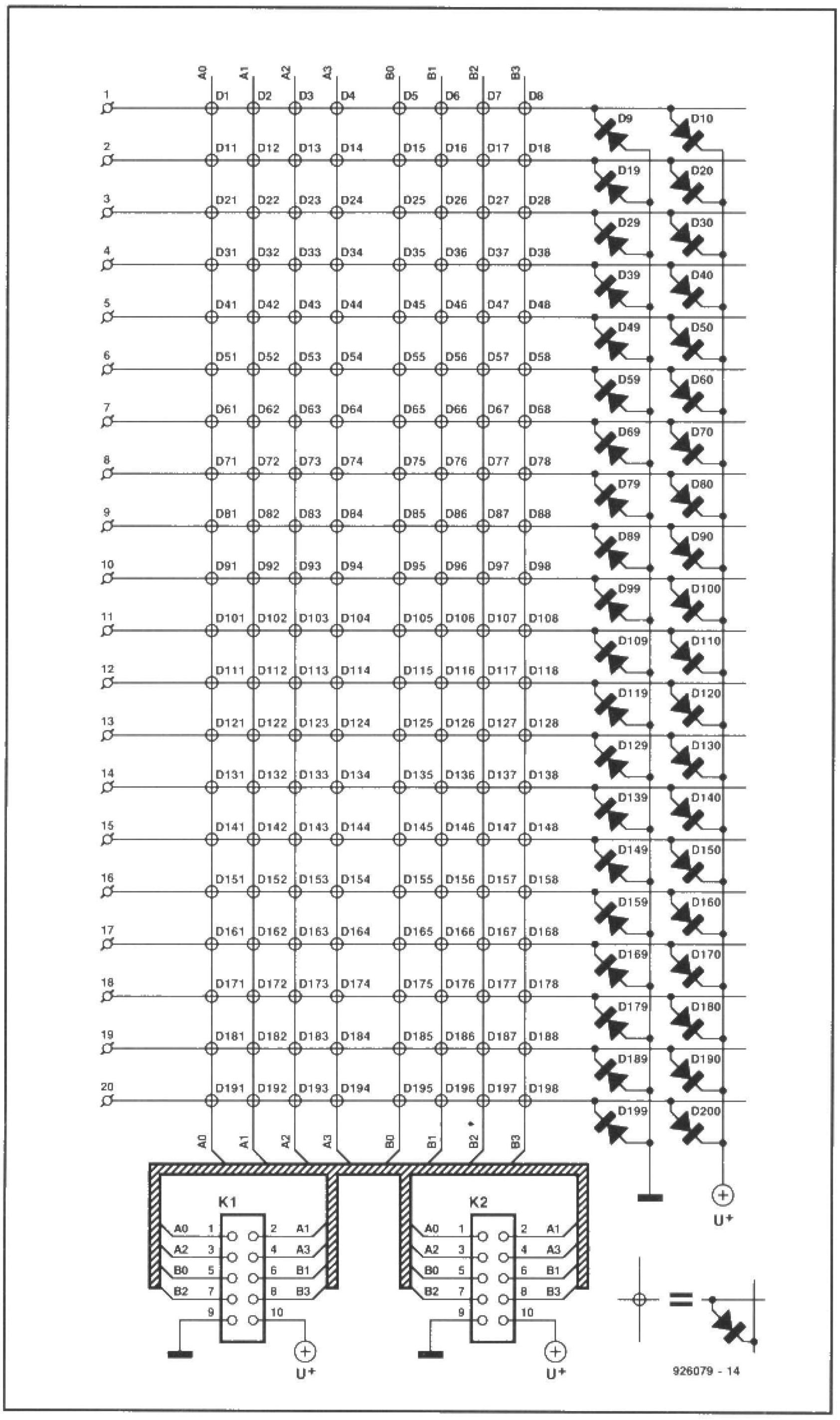


Fig. 8. Layout of the diode matrix.

The slave unit

The circuit of the slave unit, excluding the matrix, is shown in Fig. 4.

The signal from the master unit is applied across resistor R_8 via pins 9 and 10 of K_1. Transistor T_1, resistor R_7 and diode D_{11} form a voltage regulator that limits the potential across buffer capacitor C_8 to about 6.2 V. The transistor also ensures that C_8 is not discharged completely when the pulse from the master unit ceases.

The pulse across R_8 clocks monostable IC_{1a} after a delay determined by R_1C_1. In this way, IC_{1a} provides a pulse that occurs near the centre of the pulse from the master unit. To prevent the delayed pulse reaching the trigger input of IC_{1a} via IC_3 and the diode matrix, the trigger input is held high during the pulse duration by D_1 and R_2.

Monostable IC_{1b} serves two purposes: (a) to ensure that a 1 is clocked into the shift register only at the first of the eight pulses, and (b) that the shift register is reset during the pause between two pulse trains. This is achieved by making the pulse time of the monostable longer than the period of the pulses in the train and shorter than the pause between two consecutive trains. As long as IC_{1b} is triggered by the pulses, the 1 is moved on through the shift register. At the onset of the pause, IC_{1b} returns to its quiescent state and IC_2 is reset by network R_5-R_6-C_4-D_2, which also provides a power-on reset.

The eight parallel outputs of the shift register with which the bit is selected that is applied to the master unit, are linked to IC_3, which forms the switch already discussed in paragraph 1.

Every time IC_{1a} emits a pulse, one of the outputs will go low and the others high. The low output will cause a dip in the pulse from the master via the diode matrix—that is, if a diode is used for that bit.

The zener diodes in series with the outputs of IC_3 ensure that the voltage accross the two connected wires does not drop below 3.3 V (2.7 V plus 0.6 V from the matrix diode) during the current pulse from the master unit. This arrangement ensures a satisfactory power supply to the slave unit.

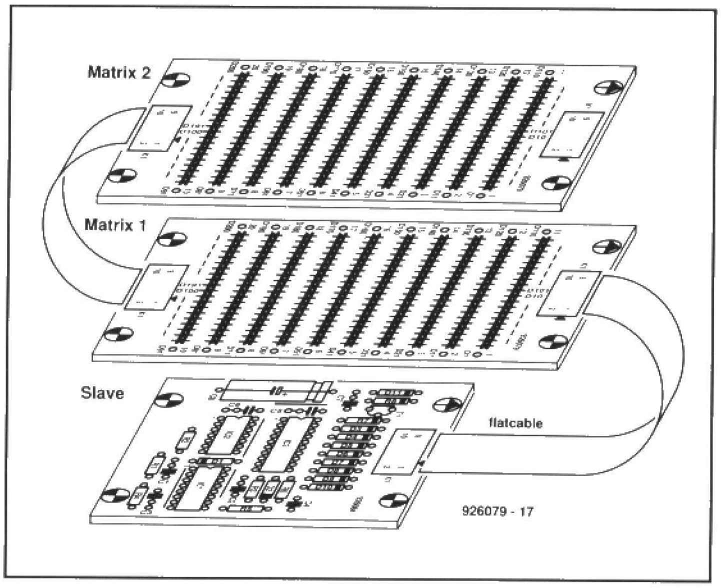


Fig. 9. How to interlink the slave and matrix boards.

PARTS LIST
Slave unit

Resistors:
R1 = 1 MΩ
R2 = 10 kΩ
R3 = 47 kΩ
R4 = 270 kΩ
R5 = 100 Ω
R6 = 100 kΩ
R7 = 390 Ω
R8 = 1 kΩ

Capacitors:
C1 = 3.3 nF
C2 = 120 \ nF
C3 = 330 nF
C4 = 470 pF
C5–C7 = 100 nF
C8 = 100 μF, 16 V

Semiconductors:
D1, D2 = 1N4148
D3–D10 = zener, 2.7 V, 400 mW
D11 = zener, 6.8 V, 400 mW
T1 = BC547B
IC1 = 74HC123
IC2 = 74HC164
IC3 = 74HC540

Miscellaneous:
K1 = 10-way flatcable connector for board mounting
Enclosure 125×49×70 mm (e.g., Type RG2 from Retex)
PCB Type 926084

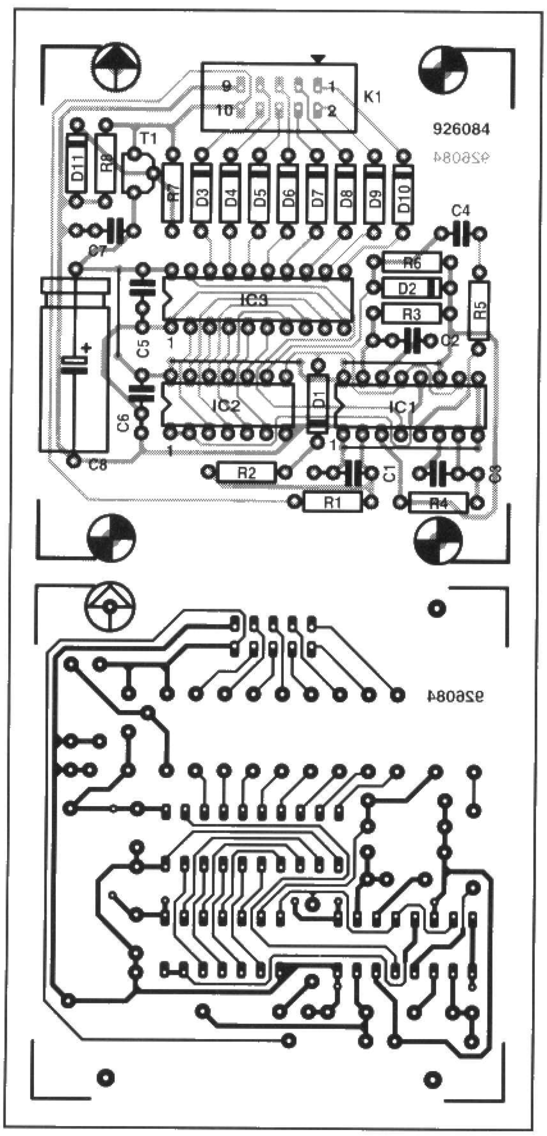


Fig. 10. Printed-circuit board for the slave unit.

Construction

The tester is constructed on three types of board: one for the master unit, one for the slave unit, and one for the diode matrix. Each matrix board allows up to 20 wires to be connected, so that a tester for 99 wires requires five matrix boards. The number of diodes required is shown in Table 2. Mount the diodes whose designation ends in a 0 or a 9 first, and only then the other diodes in accordance with the BCD code in Table 1.

The slave board and matrix boards are interlinked as shown in Fig. 9. The enclosure stated in the parts list can house one slave board and two matrix boards.

It is possible to use a spring-loaded push-button instead of a standard on/off switch on the master unit to save batteries. From a practical point of view, it is, however, better to use a standard switch in parallel with a push-button, so that in cases where you have no hand free to press the button, the standard switch can be used.

In use, connect the multicore cable as required at one end, say, to a connector box and then link the slave unit to it in accordance with the pin numbers of the connector box. Connect the master unit at the other end of the cable to **any two wires**, whereupon the display will show the pin number of the wire that is connected to the 'hot' terminal of the master unit. In this way, 'connect wire' and 'next wire' are easily identified. ■

CROSS-OVER-POINT DETECTOR

Design by T. Giesberts

Usually, the –3 dB (and –20 dB) roll-off points on the frequency characteristic of a filter are found with the aid of an oscilloscope or a millivoltmeter. Not everyone has these instruments available, however, and it is primarily for these designers that the detector described in this article is intended . Nevertheless, even if you already have a suitable oscilloscope, you will find the detector a handy addition to your workshop instruments.

In principle, the detector is simply an LED VU meter whose scale and input amplifier have been modified to facilitate the seeking of the roll-off points.

The scale is illustrated in Fig. 1. It begins at D_5 which indicates whether the signal is attenuated more than –20 dB with respect to zero level. The point at which this diode extinguishes and D_6 lights is exactly –20 dB. In the same way, the –3 dB point is exactly at the transition between D_6 and D_7. However, the transitions between D_7 and D_8 and between D_8 and D_9 are not fixed, but can be shifted by 0 dB to –1 dB, and 0 dB to +1 dB respectively. The two transitions are shifted simultaneously in such a manner that D_8 always covers a range that is symmetric around the 0 dB point. This arrangement serves two purposes. First, it allows the detector to be set to the 0 dB level of the filter on test. The range covered by D_8 is then zero, the diode is switched off (or nearly so) and a transition, which is at exactly 0 dB, ensues directly from D_7 to D_9. Note, however, that it may happen that D_7 and D_9 briefly light simultaneously: this is caused by

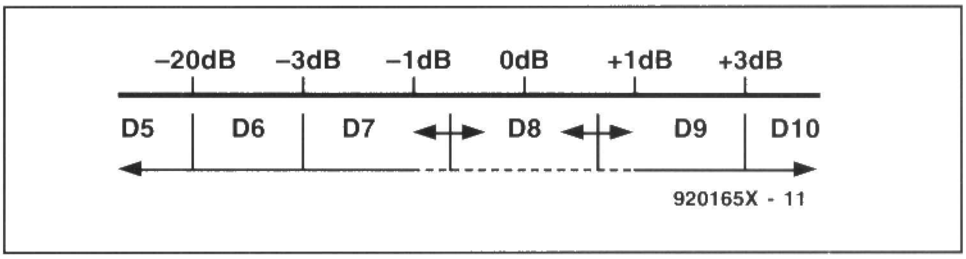


Fig. 1. The scale of the detector has a variable range around 0 dB.

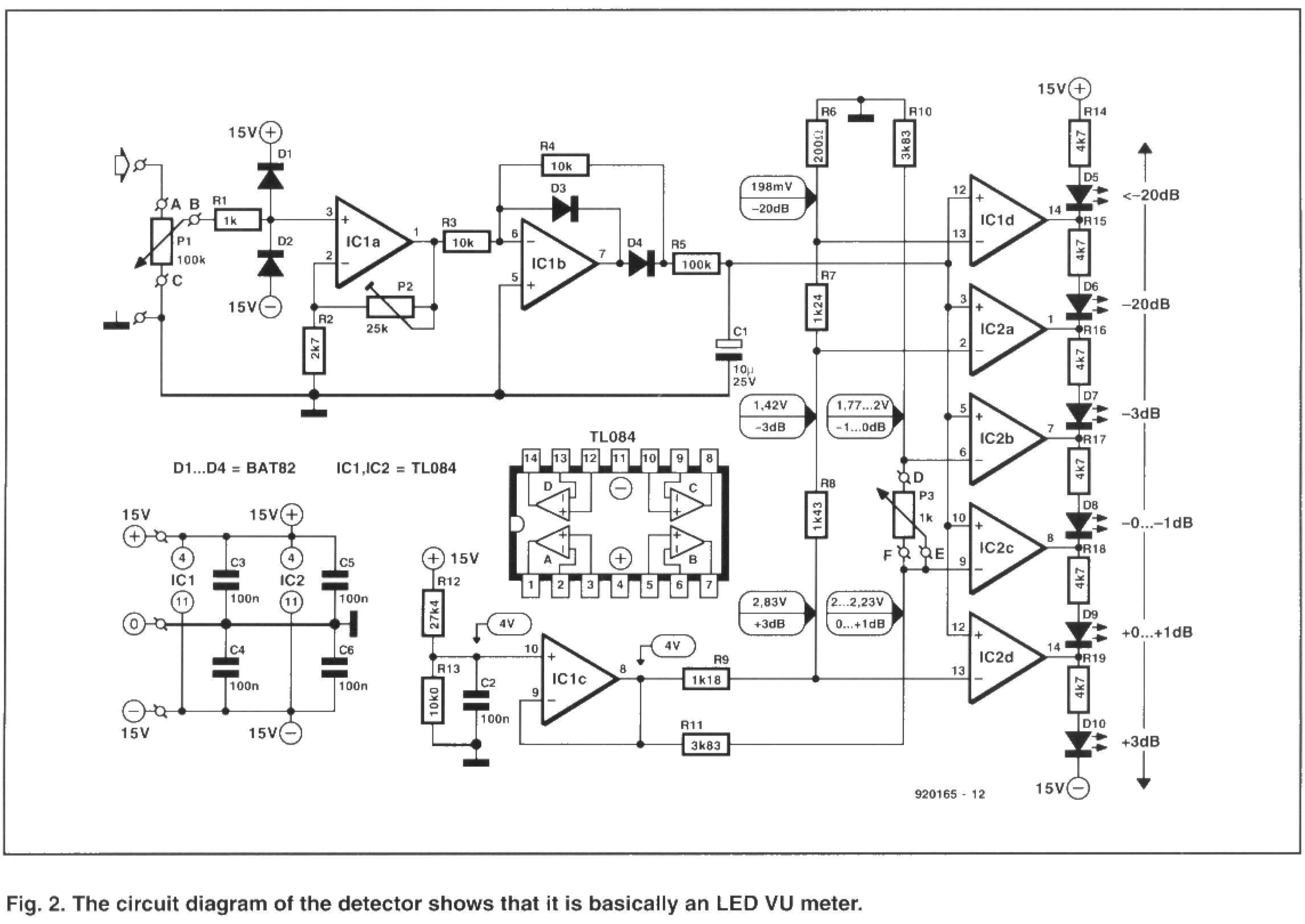


Fig. 2. The circuit diagram of the detector shows that it is basically an LED VU meter.

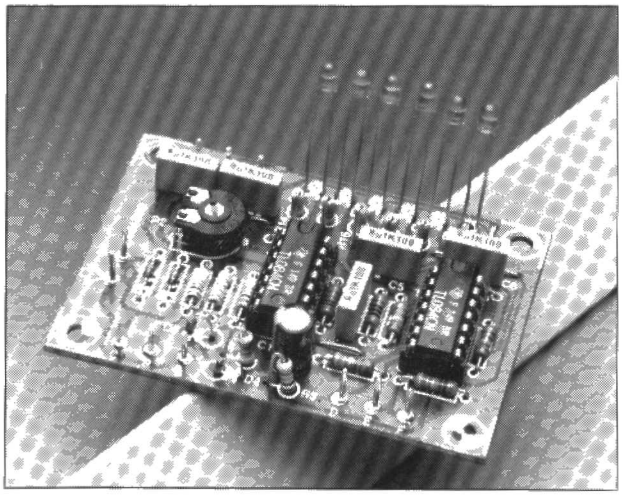
the difference in off-set voltages of the opamps. Second, it allows restricting the range covered by D_8 to, say, 0.1 dB to enable small deviations in the frequency characteristic or the onset of the roll-off to be detected. Diode D_{10} lights to show that the input level is more than 3 dB above zero.

Circuit description

The circuit in Fig. 2 is virtually that of a discrete VU meter. The function of light-emitting diodes D_5–D_{10} and the ranges they cover have already been discussed. They are driven by opamps IC_{1d} and IC_{2a}–IC_{2d}, which ensure that at any one time only one of the six diodes lights. The level at which a diode extinguishes and the adjacent one lights is determined by the potentials at the inverting (–) inputs of the opamps. The (fixed) levels at the non-inverting (+) inputs of the opamps are determined by potential divider R_6–R_9.

The variable levels for the zero range are set with voltage divider R_{10}-R_{11}-P_3, which has been designed in a manner which ensures that the levels at the inverting inputs of IC_{2b} and IC_{2c} are symmetrical around the zero level at all times. The 4-V reference voltage for the divider is provided by R_{12}-R_{13} and buffer IC_{1c}.

The input signal is applied across P_1, with which the detector is adjusted to 0. Diodes D_1 and D_2 and resistor R_1 protect the input of IC_{1a} against too high levels. The signal is amplified ×1–10 by IC_{1a}, depending on the setting of P_2, whereupon it is single-phase rectified by IC_{1b}. The resulting direct voltage is smoothed by R_5-C_1 to a level of ×0.32 the peak value of the output of IC_{1a}. Since the input level for 0 dB is 2 V, a simple calculation shows that the maximum input sensitivity is 450 (strictly, 433 mV).



Parameters

Frequency range	8 Hz–400 kHz ±1% ($P_2 = 0\ \Omega$)
	8 Hz–50 kHz ±1% (P_2 = max)
Resolution	>0.5 dB
Measuring range	–20 dB to +3 dB
Supply voltage	±15 V
Current drain	30 mA max.
Input sensitivity	450 mV

Construction and use

Although a PCB—see Fig. 3—has been designed for the detector, this is regrettably not available through our Readers' services.

The LEDs may be mounted at either side of the board. Do not forget the three wire links. To ensure an accurate indication of ±1 dB, it is essential that the value of P_3 is exactly 1 kΩ. If that is not so, R_{10} and R_{11} should be adapted in accordance with the error on P_3 (if, for instance, P_3 is 5% higher than 1 kΩ, the value of the two fixed resistors should also be 5% higher than indicated).

Most users will probably set P_2 to maximum, but if a less sensitive input can be used, this preset can be adjusted accordingly—this will also increase the bandwidth.

To use the detector unit, apply to the filter or amplifier on test a sinusoidal signal at a frequency of about 1 kHz and a level to give a filter or amplifier output of at least 450 mV r.m.s. Set P_3 to minimum (D_8 is then off) and adjust P_1 so that the display is at the transition between D_7 and D_9: either of these lights and the other extinguishes or both light faintly. That determines the 0 dB level, whereupon P_3 can be set to maximum or to an intermediate setting if required. Next, vary the frequency of the sine wave generator to find the –3 dB point(s) of the device on test. It is, of course, essential that the generator output is stable. Any doubts about that can be dispelled (or confirmed) by connecting the detector unit to the output of the generator and setting the 0 dB level at 1 kHz. Set the operating range of D_8 to about 0.1 dB and vary the frequency of the generator. The display will indicate how stable the generator output is. ■

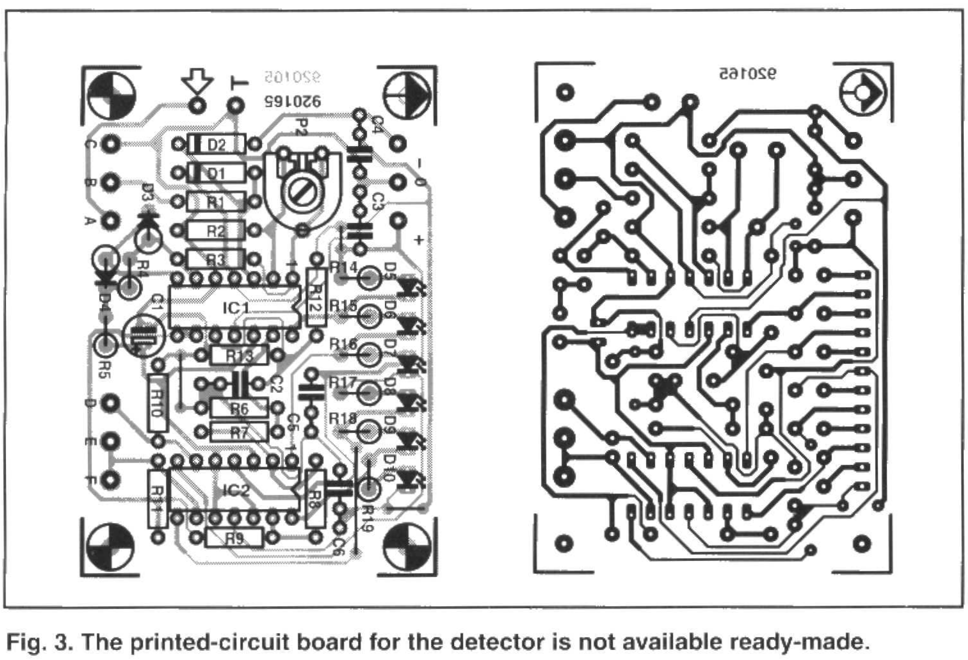


Fig. 3. The printed-circuit board for the detector is not available ready-made.

COMPONENTS LIST

Resistors:
R1 = 1 kΩ
R2 = 2.7 kΩ
R3, R4 = 10 kΩ
R5 = 100 kΩ
R6 = 200 Ω, 1%
R7 = 1.24 kΩ, 1%
R8 = 1.43 kΩ, 1%
R9 = 1.18 kΩ, 1%
R10, R11 = 3.83 kΩ, 1%
R12 = 27.4 kΩ, 1%
R13 = 10.0 kΩ, 1%
R14–R19 = 4.7 kΩ preset
P1 = 100 kΩ, log potentiometer
P2 = 25 kΩ preset
P3 = 1 kΩ potentiometer

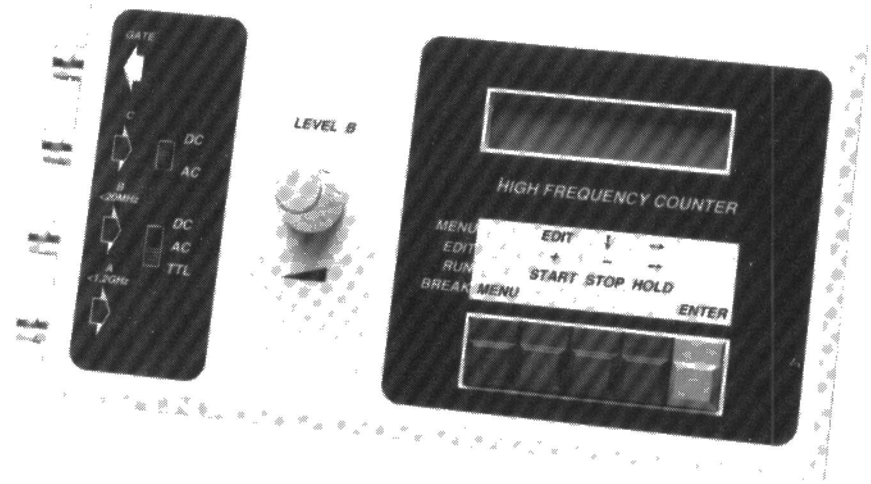
Capacitors:
C1 = 10 µF, 25 V, radial
C2–C6 = 100 nF

Semiconductors:
D1–D4 = BAT82
D5–D10 = LED, high efficiency
IC1, IC2 = TL084

1.2 GHz MULTIFUNCTION FREQUENCY METER

PART 2: USER MENU DESCRIPTION

Design by B. C. Zschocke



After the circuit description and the construction guidelines given last month we now turn to the way the multifunction counter is operated via the extensive menu. Basically, the user entry function builds a string of command characters that are sent to measurement subroutines contained in the control program of the instrument. As you will recall from the first instalment, the frequency meter is based on a 80C32 microcontroller which runs a control program contained in an EPROM. This program was developed by the author using an assembler. The command character string is stored internally, and is available to the instrument as a kind of default message which contains all relevant data and parameters to perform a particular type of measurement (of which there are quite a few — see later). How the command string is built up is discussed here. If you have already built the counter, now is a good time to switch it on and explore the various menu options and instrument parameters.

The menu

The menu entries required to set up a particular type of measurement are analogous to following, from the top to the bottom, the options shown in the menu overview in Fig. 8. The overview shows six basic functions related to measurement modes:

- frequency, 1/frequency and rpm (revolutions per minute) measurement;
- pulse counting on channel A and B;
- time measurement;
- pulse (frequency) generator;
- timer;
- up/down (manual) counter on channel C.

Simply start at the top of the diagram, from the 'reset' box, and find your way down to the 'entry' box, via the appropriate functions and parameters. As an example, let us set up an rpm measurement. The menu selections are:

MENU → FUNCTION: rpm → SELECT INPUT: Channel B → gate time: 1 min. Start: on 'start' key → Mode: continuous → Settings: with period analysis; no intermediate results; buzzer off → Entry: exit & start.

Most menu options shown in the overview correspond to the actual indication on the LC display. In a few instances, however, the LCD indications have been shortened, for example, 'press' for 'pressed' and 'interm.' for 'intermediate'. All this will be fairly evident, however, and is not likely to cause problems in practice. The keys are arranged as follows on the instrument front panel (from the left to the right): MENU (S6); START (S5); STOP (S4); HOLD (S2); ENTER (S3).

Measurement functions are selected as follows using the above keys: after selecting MENU from the start options, the STOP key is used to select a particular measurement function (refer back to Fig. 8). The top line on the LCD shows the available functions, and the bottom line the selected function. ENTER key is pressed to confirm the required function. This takes you to the next menu option. If, however, you wish to use the default function rather than the one selected, simply press the HOLD key rather than the ENTER key. This allows you to make a new selection from the functions or options.

An exception is formed by the SETTINGS (see Fig. 8) submenu, which presents you with two options. The one you want is selected by a toggle function under the control of the EDIT key (for example: buzzer on/buzzer off).

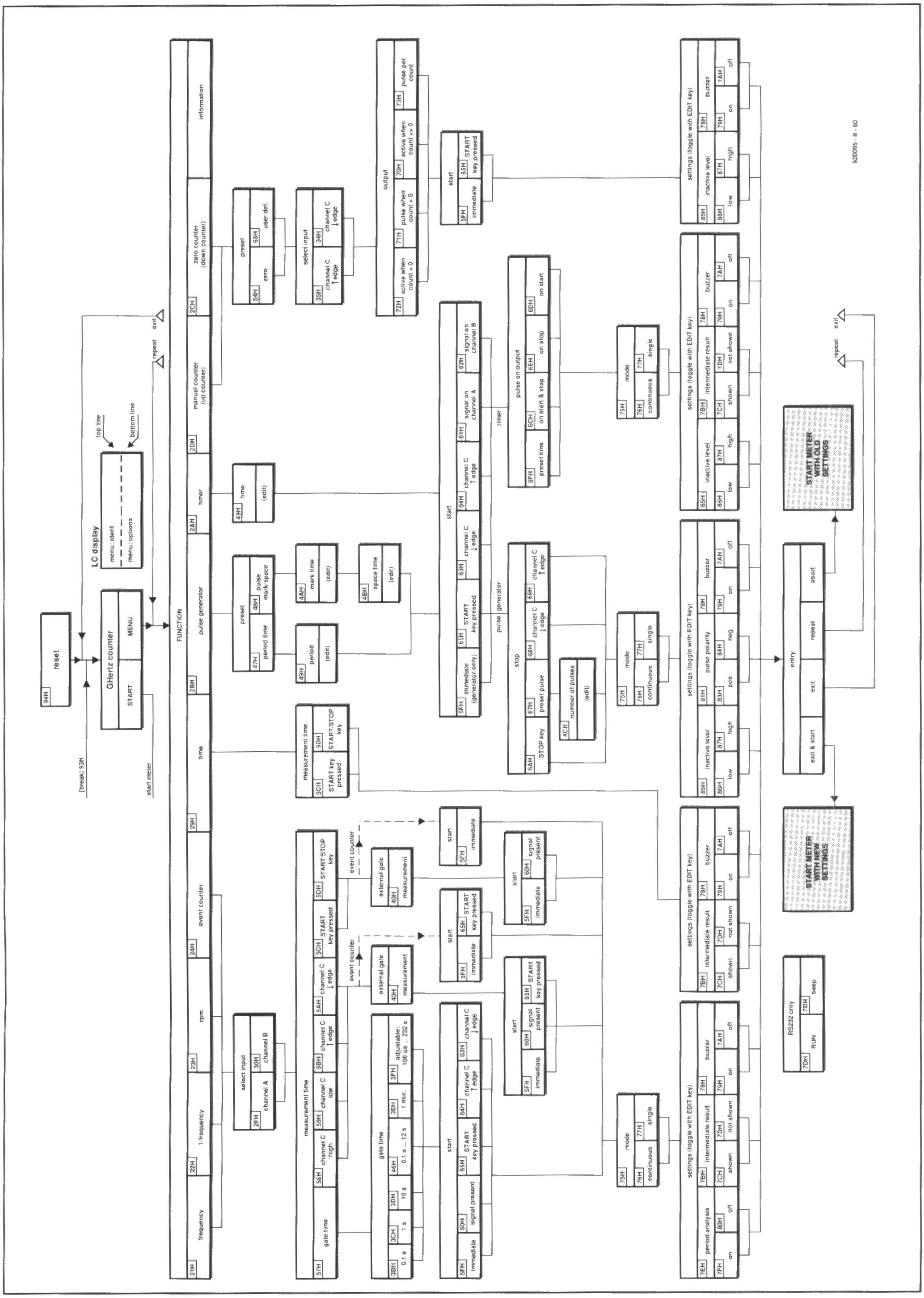
Special points

During the selection of a function or option, the default settings may be recalled by pressing the MENU key. The default function or option is also shown as the first selection. If this is not possible, for instance, after the measurement mode has been changed, the left-most function shown in Fig. 8 appears. After switching on, the default mode is frequency measurement on channel B. Pressing START and ENTER simultaneously ends the entry mode, and starts the actual measurement.

Where the menu overview (Fig. 8) indicates 'adjustable', the lower line of the LC display shows a number. This number, usually a zero or a value taken from the last entry or measurement, may be changed by the user by going to the 'edit' mode via the START key. Next, the number appears with leading zeroes, an arrow at the start of the line to indicate that you are in EDIT mode, and a cursor in the form of an underscore (_) under the first digit at the far left. The START (+) and STOP (–) keys are used to increase and decrease the digit value respectively. The HOLD key is used to move the cursor through the number, and put the cursor under the digit to be changed. After the last digit, the cursor jumps back to the first. In this way, the user-defined value is set up, and confirmed by pressing the ENTER key (which takes you out of the 'edit' mode). Note that the original value can not be recalled after the ENTER key has been pressed: the value you have set is final!

Practical experience has shown that the finding your way through the various menus takes some getting used to, but in general will be easy to learn. However, you may wonder at this point what is behind all these functions and options offered by the instrument. The descriptions below provide the answers. Please also refer to Fig. 8 to follow the order in which the functions are discussed.

Fig. 8. (Opposite) User menu overview.


reset
94H
[break] 93H
GHertz counter
START
MENU
start meter
LC display
menu: ident
menu: options
top line
bottom line
repeat
exit
FUNCTION
21H frequency
22H 1:frequency
23H rpm
24H event counter
29H time
2BH pulse generator
2AH timer
2DH manual counter (up counter)
2CH zero counter (down counter)
information
select input
2FH channel A
30H channel B
measurement time
57H gate time
58H channel C high
59H channel C low
5BH channel C ↑edge
5AH channel C ↓edge
5CH START key pressed
5DH START/STOP key
gate time
3BH 0.1 s
3CH 1 s
3DH 10 s
46H 0.1 s ... 12 s
3EH 1 min.
3FH adjustable: 100 us ... 232 s
external gate
40H measurement
event counter
start
5FH immediate
60H signal present
65H START key pressed
64H channel C ↑edge
63H channel C ↓edge
measurement time
5CH START key pressed
5DH START/STOP key
preset
47H period time
48H pulse mark/space
49H period
(edit)
4AH mark time
4BH space time
49H time
preset
54H zero
55H user def.
select input
35H channel C ↑edge
34H channel C ↓edge
output
72H active when count = 0
71H pulse when count = 0
70H active when count <> 0
73H pulse per count
5FH immediate (generator only)
65H START key pressed
63H channel C ↓edge
64H channel C ↑edge
61H signal on channel A
62H signal on channel B
timer
pulse generator
stop
6AH STOP key
67H preset pulse
68H channel C ↓edge
69H channel C ↑edge
4CH number of pulses
pulse on output
6FH preset time
6CH on start & stop
6EH on stop
6DH on start
mode
75H
76H continuous
77H single
settings (toggle with EDIT key)
7EH period analysis
7FH on
80H off
7BH intermediate result
7CH shown
7DH not shown
78H buzzer
79H on
7AH off
85H inactive level
86H low
87H high
81H pulse polarity
83H pos
84H neg
entry
exit & start
exit
repeat
abort
START METER WITH NEW SETTINGS
START METER WITH OLD SETTINGS
RS232 only
70H RUN
7DH beep
920095 - II - 60

Function: frequency
Frequency measurements are carried out via channel A or channel B. Channel A (with prescaler) allows measurements to over 1 GHz, while channel B is suitable for input signals up to about 25 MHz. Channel B is also suitable for measuring DC-coupled signals in the mHz (milli-hertz) range. For optimum precision, the gate time is measured along with the rate of change of the input signal. The resulting frequency is calculated with the aid of a 64-bit ALU (arithmetic logic unit). This measurement method also allows 'non-standard' or external gate times to be used, which is essential for pulsed signals.

Function: 1/frequency
This measurement mode serves to indicate the period of the measured signal. The measurement principle is the same as that used for frequency measurement, except that the ALU calculates the reciprocal value. Hence the perhaps unusual indication of a gate time rather than a number of periods.

Function: revolution counter
The rev./min measurement is also based on the frequency measurement principle. Note, however, that the result is indicated in revolutions per minute rather than hertz.

Function: pulse counter
In this mode the instrument counts the pulses that occur on channel A or channel B. The duration of the measurement may be limited by a gate time. It should be noted that the gate times are not accurate. This is caused by the nested interrupt structure of the 80C32 processor. Do not, therefore, calculate the frequency on the basis of the pulse counter result and the gate time, since this will yield inaccurate results.

Function: time
The time measurement mode may be compared to a chronograph or stopwatch. To make sure that the start and stop keys are denounced, a keypad scanner has been realized with the aid of an internal clock generator. This generator limits the accuracy of the stopwatch to a little less than 0.1 s. During the measurement, the GATE output is made logic high.

Function: timer
The timer mode allows you set GATE output times to over 1 second in 1-μs steps. Depending on your choice (made via the menu), the timer starts on the presence of a signal edge at the channel A or channel B input, a high-to-low or low-to-high transition at the channel C input, or the depression of the START key.

Function: pulse generator
The pulse generator, or frequency generator, is an extended version of the timer function. This mode allows you to generate single pulses, as well as pulse trains with almost any combination of pulse duration, mark/space (pulse/pause) ratio and number of pulses. The number of periods can only be processed if the period length (pulse length and pause length) is greater than 256. Frequencies can be generated by entering their periods ($1/f$). The pulses are available at the GATE output. The 'start on' options are the same as those for the timer.

Function: information
Select this option to display information on copyright and current software version.

Select input: channel A
Channel A serves to measure high frequencies (up to 1.2 GHz). It is not suitable for low frequencies because of the input capacitors and the reduced sensitivity of the prescaler IC below 20 MHz or so. Higher frequencies are, however, amplified and divided by 64.

Select input: channel B
Channel B serves to measure signals at frequencies of a few millihertz (mHz) to about 25 megahertz (MHz). Switch S9 allows this channel to be either TTL compatible, or AC or DC coupled with a preamplifier. The amplification is adjusted with potentiometer P3.

Select input: channel C
Channel C is either TTL-compatible or AC coupled, as selected by switch S8. The sensitivity of this input can be increased to less than 1 V by adjusting preset P4 in the AC-coupled input circuit.

Measurement time: gate time
In this mode, the measurement time is determined by the gate time generator. You may choose between a number of fixed gate times (0.1 s, 1 s, 10 s, 1 min.), a 'sliding', or a user-defined gate time. When 'sliding' gate time is selected, the first measurement is carried out with a gate time of 0.1 s. The gate time is doubled every successive measurement, until it equals 12.8 s. In the adjustable gate time mode, you are not prompted to enter a lower limit. It is recommended to make the gate time equal to an even multiple of the period of any interfering signal(s), or a modulating signal, if present. It should be noted that the gate times are not accurate (see under 'pulse counter' above). Fortunately, the deviation is small at about 100 μs, which will be negligible in most cases.

Measurement time: channel C high (low)
This mode allows you to measure when the signal level at the channel C input is high (or low). The gate time corresponds roughly to the time channel C is high (low). Before the measurement, channel C must be low (high), since the start of the measurement is recognized by the relevant signal edge.

Measurement time:
- channel C ↑ edge - START/STOP
- channel C ↓ edge - START/STOP
In this mode, an low-to-high (L-H) edge (or a H-L edge) on channel C start the measurement, while a further L-H (or H-L) edge stops it. The gate time corresponds roughly to the time between two edges.

Measurement time: START key pressed
In this mode, the gate time equals the time the START key is pressed.

Measurement time: START/STOP key pressed
In this mode, the gate time starts when the START key is pressed, and stops when the STOP key is pressed.

External gate: measurement
Notification to the user that the gate time is not furnished by the gate time generator, but by a measurement on channel C, or a key action.

Start: immediate
This option is self-evident: the measurement starts immediately.

Start: signal present
Selecting this option forces the instrument to wait until a signal is detected at the input. If the gate time is determined by channel C or by key action, the instrument waits on the signal first, then either on the condition set up for channel C, or on the key action.

Start: START key
Selecting this option causes the measurement to start the measurement the instant the START key is pressed.

Start: channel C ↑ edge; channel C ↓ edge
The measurement starts on the L-H (H-L) transition (edge) of the signal applied to channel C.

Mode: continuous/single
In continuous mode, the measurement is repeated until the user presses BREAK (i.e., the MENU and ENTER keys simultaneously). The 'single' setting is self-evident.

Settings: period analysis

The period analysis option is a special feature of the frequency meter. The accuracy of a frequency measurement can be increased by setting a gate time equal to an even number multiple of the period of the measured signal. This principle, which is essential for very low frequency measurements, will be given further attention in a separate article to be published soon. After the start of the measurement, the software idles in a loop until the first period is counted. Next, the gate time generator is started. When the gate time proper has elapsed, the software enters another loop, and waits until the current period of the measured signal is finished. A couple of programming tricks allowed the loop to be reduced to four machine cycles, which means that the period analysis has an accuracy of about 8 μs. This, in turn, results in an accuracy of five digits (max.) per second gate time.

The period analysis option is not useful with frequencies above 100 kHz or so. Since both the period analysis and the 'signal present' option wait for the start of a period, it makes little sense to use them simultaneously. Indeed, their combination only lengthens the measurement, particularly in the case of low frequencies.

Accurate measurement of low frequencies, particularly those in the millihertz range, is only possible with the period analysis option enabled. The lengthening of the gate time to at least one period may cause a low-frequency measurement to last fairly long, irrespective of the set gate time. The setting displayed after pressing the START key may be changed with the aid of the EDIT key.

Settings: intermediate results

With most types of measurement there exists the possibility to display results during the actual measurement. This is achieved by extending the gate time measurement routine in a manner that the instrument attempts to store the current counter state and the gate time elapsed so far, in the secondary register bank. This is done roughly every two seconds. When the attempt fails, the software waits a further 2 seconds. Next, the frequency is calculated from the stored counter states. There are, however, two limitations to this: first, with high frequencies, attempts to record a valid combination of current counter state and gate time may fail all the time; second, the error in the displayed measured value increases as the measured frequency decreases.

On the display, an intermediate value is indicated by a diamond (◊). Pressing the HOLD key 'freezes' the intermediate value on the display, until the final result is available. The 'intermediate result' setting shown after the START key is pressed may be changed (toggled) with the EDIT key.

Settings: buzzer

As already mentioned, the instrument is capable of generating tones under software control. These tones are produced by a passive buzzer, which sounds at the start and the end of a measurement. While it generates a tone, the processor is not available for other tasks, including interrupt handling. The tone generator may be switched off for silent measurements, or to prevent slowing down of the interrupt processing. The buzzer setting displayed after pressing START may be changed (toggled) by pressing the EDIT key.

Pulse on output

The GATE output on the instrument is logic high (1) during the gate time of a measurement, and (2) as long as the counter is waiting for a signal edge (options: period analysis; signal present).

Pulse on output: preset time

The instrument prompts you to enter a timing period.

Pulse on output: on stop

At the end of the timing period set up by the timer function, a 1-μs long pulse appears at the GATE output. This option is only useful with relatively long times, since the delay between the start of the timer and the actual start of the timing period can not be defined, and may be about 100 μs.

Pulse on output: on start

A 1-μs long pulse appears at the GATE output on the start of the period set for the timer. This option is only useful when the user is alerted (by the buzzer) that the timing period is finished.

Pulse on output: on start and stop

In this mode the GATE output supplies a 1-μs pulse at the start and the end of the timing period. When a timing period of 1 μs is set, the output supplies only one pulse.

Settings: inactive level

This option allows you to define whether the output, when inactive, is logic high or logic low. The inactive level selection has no effect on the basic mode of the instrument, or during menu entry.

Preset time: period time

You are prompted to enter a pulse period at a resolution of 1 μs. The value entered is used by the software to generate a space duration and a mark duration ('space' = pulse inactive level; 'mark' = pulse active level). The mark and space times are made equal if the programmed period is a whole number, while they differ by 1 μs if the period is not a whole number. The smallest period that can be programmed is 4 μs (250 kHz).

Preset time: pulse mark/space

This menu option allows you to assign individual durations to the mark and the space time of a pulse.

Stop: STOP key

The pulse generator stops when the STOP key is pressed.

Stop: preset pulse

Apart from the continuous pulse train mode, you have the possibility to program the number of pulses after which the generator switches off. Owing to the limitations of the software, this is only possible if either the mark or the space duration is greater than 256 μs.

Stop:
- channel C ↑ edge
- channel C ↓ edge

Depending on the option chosen, the frequency generator (timer) stops when a positive (↑) or negative (↓) pulse level is applied to the channel C input.

Settings: pulse polarity

This submenu allows you to define the mark (active pulse level) as a negative pulse level. The level of the space is not taken into account.

Function: manual counter/zero counter

In contrast with the function 'pulse counting', every count event is displayed in this mode. Counting can be in the 'up' or 'down' direction. Provision has also been made to count into the negative range. The manual and zero counter differ only in respect of the effect of a signal edge on channel C. In the zero counter mode, each H-L edge (or L-H edge, depending on your selection) causes the counter value to be decreased by one. By contrast, the manual counter is increased by one on every H-L or L-H signal edge detected at the channel C input.

Preset: zero/user defined

The start value of the manual and zero counter can be set to zero or a user-defined value, which can be any positive number.

Output: active when count = 0

The output goes active when the counter reaches state 'zero'.

Output: active when count ≠ 0
The output goes active when the counter state is not zero.

Output: pulse when count = 0
The output supplies a 1-µs pulse when the counter reaches state 'zero'.

Output: pulse per count
The output supplies a pulse on every counter state change.

Miscellaneous
In addition to the key combination 'BREAK' (MENU and ENTER pressed simultaneously), pressing ENTER and START simultaneously allows you to load a start value into the manual and zero counters. Furthermore, the combination ENTER and STOP ends the counting process just like a 'BREAK'. The START and STOP keys may be used to increase and decrease the counted value respectively in steps of one count.

Status indications and other reports

During the measurements, the instrument produces a number of status indications on the display. An icon that indicates the measurement function is shown in the upper left-hand corner of the LCD, followed by letter of the channel letter (A, B or C) on which the measurement is taking place. Next come an indication about the way the gate time is determined, and the current state at the end of the line. The meaning of the letters and symbols is as follows:

A	measurement on channel A.
B	measurement on channel B.
GT	gate time supplied by gate time generator.
C+	gate time equals high phase on channel C.
C–	gate time equals low phase on channel C.
C↑	gate time started and stopped on L-H edge.
C↓	gate time started and stopped on H-L edge.
TA	gate time determined by pressing START key.
SS	gate time started with START key and stopped with STOP key.
ready	instrument waiting for start condition.
waiting	instrument waiting for signal (edge) on channel.
running	instrument busy performing measurement.
stopped	measurement finished.

The second line on the LCD indicates the measurement result or the intermediate results. The signs that appear have the following meaning:

◊	intermediate value shown.
*	final result shown.
→	EDIT mode — value may be edited.

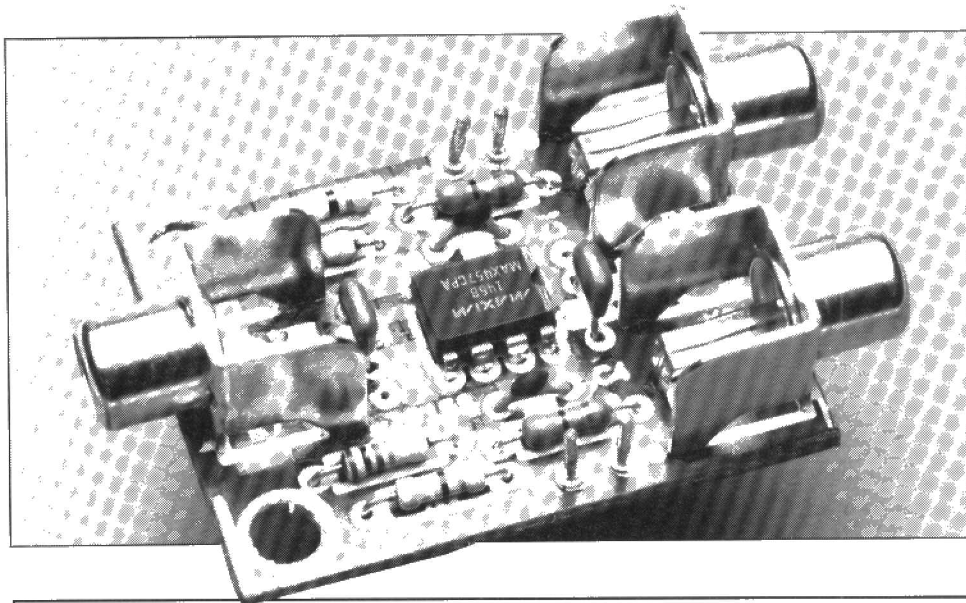
Finally, the error reports:

Counter overflow: the total number of pulses counted at the input has exceeded 2^{32}.
Gate time overflow: a gate time greater than 2^{32} µs has been set externally.
Result overflow: the result calculation yields an overflow.
Period too short: a too short period was entered, or the sum of the mark and the space time is too short.

Next month's instalment will discuss the functions of the serial port on the instrument. As already mentioned in part 1, the measurement principles used in the counter will be discussed in a separate article. ❑

DUAL VIDEO AMPLIFIER

A good video amplifier has a bandwidth considerably greater than that of the average video signal. Furthermore, it is utterly stable, and provides input and output impedances that match directly to coax cable. Phew! What requirements! Well, this article describes such an amplifier, based on Maxim's MAX457, which contains two very fast CMOS opamps. Applications: an ultra-compact video splitter/crosspoint amplifier, or a flash D-A converter driver.



Design by J. Sonderbrink

THE two amplifiers contained in the MAX457 are unity-gain stable video amplifiers capable of driving 75-Ω loads with a –3-dB bandwidth of no less than 70 MHz. They are marked by a small input capacitance (typ. 4 pF), an input bias current of 100 pA, and a high isolation between amplifiers (typ. 72 dB at 5 MHz). Ideal, therefore, for building a top-performance video splitter/amplifier from a minimum of components, or, indeed, a drop-in amplifier for almost any wideband application up to about 70 MHz.

As shown in the circuit diagram of Fig. 1, the amplifiers operate from a ±5 V symmetrical supply. Power consumption is of the order of 350 mW. Only a handful of external components are required to put the MAX457 to work. Here, the amplifiers are dimensioned for a voltage gain of ×2 at a load impedance of 150 Ω by using 1kΩ05 and 1-kΩ feedback resistors (R1-R2 and R4-R5). Table 1 shows the relation between the closed loop gain, bandwidth, optimum load impedance and the values of R1 and R2.

The small capacitor (C3; C4) between the output and the –input of each amplifier serves to prevent peaking at high frequencies. Peaking could be caused by the (small) input capacitance of the amplifier in combination with the relatively high impedance of the feedback resistors when the gain is on the low side. At 50 MHz, for instance, the feedback resistors cause a substantial phase delay, which can be largely eliminated by adding C3. At

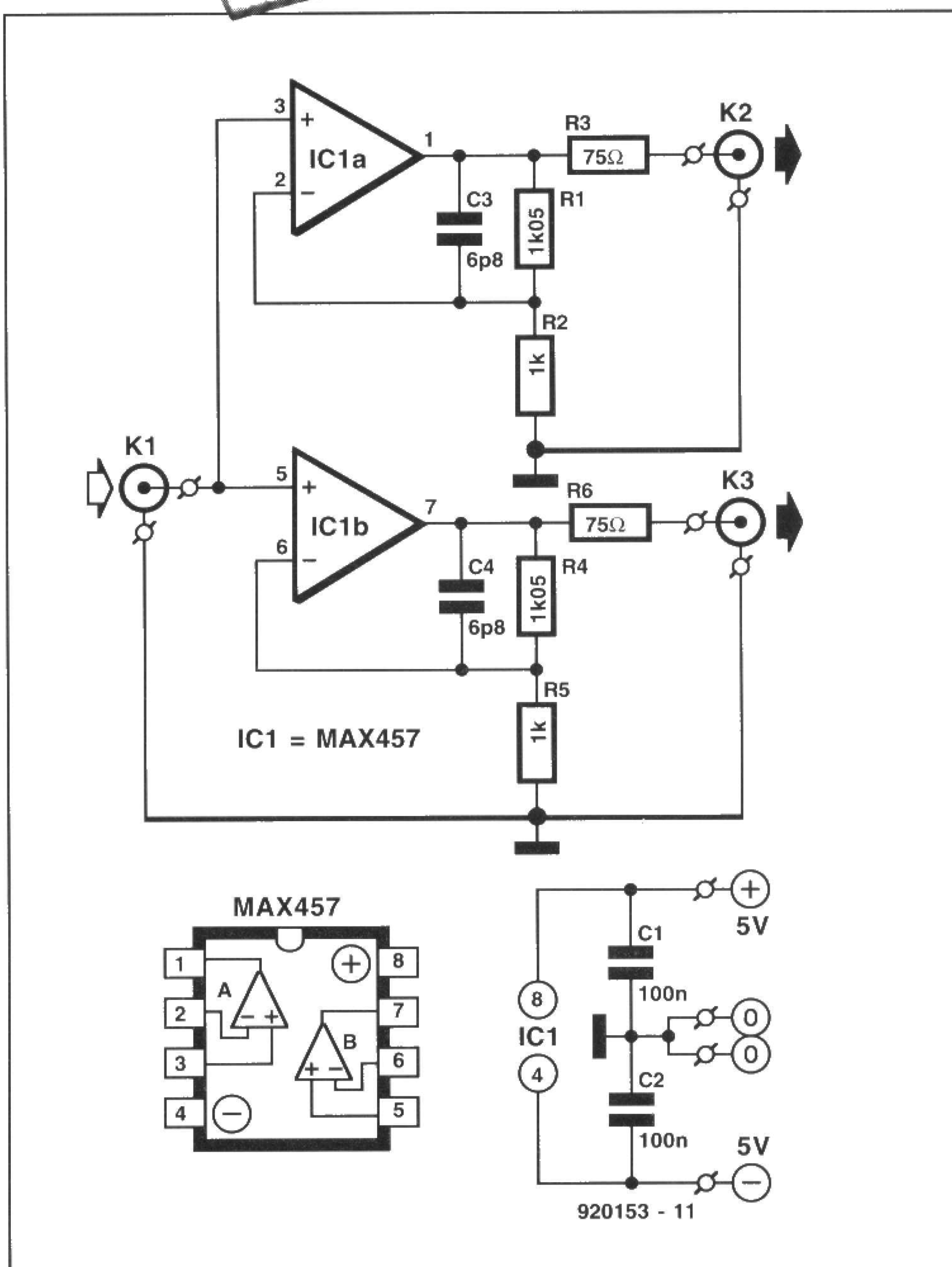


Fig. 1. Circuit diagram of the dual video amplifier: a standard application of the MAX457.

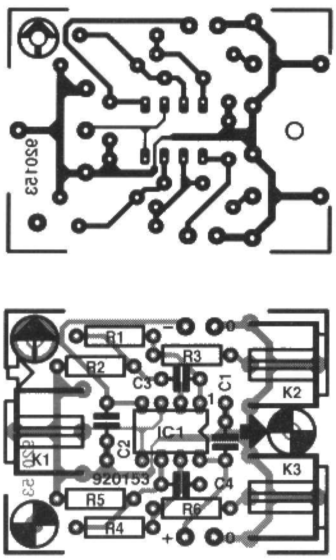


Fig. 2. Single-sided printed circuit board for the video amplifier.

higher closed-loop gains (say, x5 or more), C3 serves little purpose and should be omitted.

To ensure that the amplifier does not oscillate, the load resistor (R3; R6) should be nominally $75A_{VCL}$ (ohms) where A_{VCL} is the closed-loop gain (see Table 1). Observing this rule will result in minimum overshoot and ringing in the output signal. It is generally safe to use loads smaller than $150A_{VCL}$.

The optimum load impedance of the amplifiers as shown here is 75 Ω. When the input is driven by a coax cable, K1 should be shunted by a 75-Ω resistor.

COMPONENTS LIST

Resistors:

2	1kΩ05	R1;R4
2	1kΩ	R2;R5
2	75Ω	R3;R6

Capacitors:

2	100nF	C1;C2
2	6pF8	C3;C4

Semiconductor:

1	MAX457CPA	IC1

Miscellaneous:

3	phono socket for PCB mounting	K1;K2;K3
1	metal enclosure, e.g., Hammond 1590LB	

Construction

Little needs to be said of the construction since that is extremely simple when the printed circuit board shown in Fig. 2 is used. Connectors K1 and K2 are RCA-style phono sockets for PCB mounting. In view of the high frequencies involved, the amplifier is best housed in a small metal enclosure. A suggested type is given in the components list. ■

Table 1.
Gain and load resistor selection

Gain A_{VCL}	f_{-3dB} (MHz)	R1 (Ω)	R2 (Ω)	R_{LOAD} (Ω)
1	70	39	1000	75
2	50	1050	1000	150
5	40	4170	1000	390
10	25	9420	1000	750

Source:

MAX457 dual CMOS video amplifier, Maxim datasheet.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086, U.S.A. Telephone: (408) 7377600. Fax: (408) 7377914.

Maxim Integrated Products (UK) Ltd., 21c Horseshoe Park, Pangbourne, Reading RG8 7JW. Telephone (0734) 845255.

CONVOLUTIONAL AND BLOCK CODES FOR MULTIPLE ERROR DETECTION

By Brian P. McArdle

Introduction

The development and widespread use of data communications over recent years means that methods of error detection and correction have become more sophisticated. It is no longer sufficient for a code to be able to correct one error per block.

The purpose of this article is to review the methods for multiple error detection. It is assumed that the reader is familiar with the basic ideas of Coding Theory. A simple overview of the (7,4) Hamming Code is given in Appendix 1.

In the article it is assumed that syndrome decoding is in use unless otherwise stated. This requires some explanation. In general, an encoding operation can be represented as a matrix. The original r data bits are transformed into n bits that are, in turn, transmitted or stored.

$$\begin{bmatrix} g_{11}\, g_{12}\, g_{13} \cdots\cdots g_{1r} \\ g_{21}\, g_{22}\, g_{23} \cdots\cdots g_{2r} \\ \cdots\cdots\cdots\cdots\cdots\cdots \\ \cdots\cdots\cdots\cdots\cdots\cdots \\ g_{n1}\, g_{n2}\, g_{n3} \cdots g_{nr} \end{bmatrix} \begin{bmatrix} x_r \\ x_{r-1} \\ \cdots \\ \cdots \\ x_1 \end{bmatrix} = \begin{bmatrix} y_n \\ y_{n-1} \\ \cdots \\ \cdots \\ y_1 \end{bmatrix}$$

$$G{\cdot}\boldsymbol{x}=\boldsymbol{y}. \qquad \text{[Eq. 1]}$$

Each y_j is a combination of the r bits of the input block. The individual blocks can be considered as n-dimensional vectors or as polynomials of degree $(n-1)$ (see Appendix 3). The decoding operation is more than just the reverse of encoding. It must reproduce the original data bits but it must also check the validity of this data. If $\boldsymbol{y}$ is corrupted during transmission, it can be rewritten as $(\boldsymbol{y}+\boldsymbol{e})$, where $\boldsymbol{e}$ is the error vector. The decoding operation uses a parity check matrix H (discussed in Section 3) to calculate a syndrome as follows:

$$H{\cdot}(\boldsymbol{y}+\boldsymbol{e})=H{\cdot}\boldsymbol{y}+H{\cdot}\boldsymbol{e}=\boldsymbol{s}. \qquad \text{[Eq. 2]}$$

However, the check matrix is chosen such that $H{\cdot}\boldsymbol{y}=\boldsymbol{0}$, which results in

$$H{\cdot}\boldsymbol{e}=\boldsymbol{s}, \qquad \text{[Eq. 3]}$$

where $\boldsymbol{s}$ has dimension $(n-r)$, which is the number of check bits added to the original data block. Thus the operation does not deduce $\boldsymbol{e}$ directly as may have been expected. A particular syndrome must be matched to a particular error combination. Obviously, the set of possible syndromes is the effective limit on the suitability of a code. The total number of possible syndromes is $2^{(n-r)}$, whereas the total number of data blocks is 2^r. The total number of code words is the same as the number of data blocks, 2^r. Each data block has its corresponding check bits and, consequently, the check bits are not independent of the data bits. The generation and interpretation of a syndrome are the error detection and correction parts of any decoding operation. To detect t errors in a block of size n, the code must be able to identify ${}^nC_t=n!/[t!(n-t)!]$ different combinations of the t errors. This figure, in order to allow for the full range of errors from no error to t errors, becomes $\sum_{j=0}^{t} {}^nC_j$. There are other forms of decoding (for instance, Viterbi Algorithm for convolutional codes), but these are not discussed in this article. The two main methods of coding, convolutional and block codes, are explained in the following three sections.

2. Convolutional codes

Consider the arrangement of Fig. 1. This is a typical convolutional encoder called a Hagelbarger Code. It does not require the division of the sequence of data bits into separate blocks of specific lengths where the individual blocks are encoded. The check bits are generated according to the equation

$$c_n=(d_{n+4}+d_{n+8}) \bmod 2 \qquad \text{[Eq. 4]}$$

and are transmitted before the corresponding

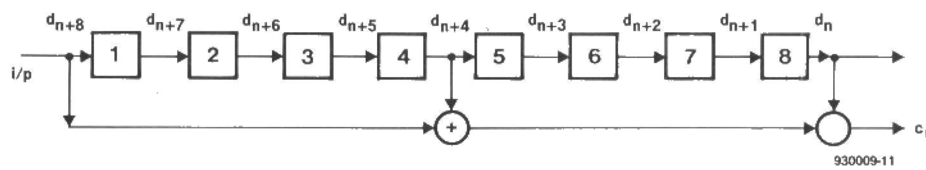


Fig. 1. Hagelbarger convolutional encoder.

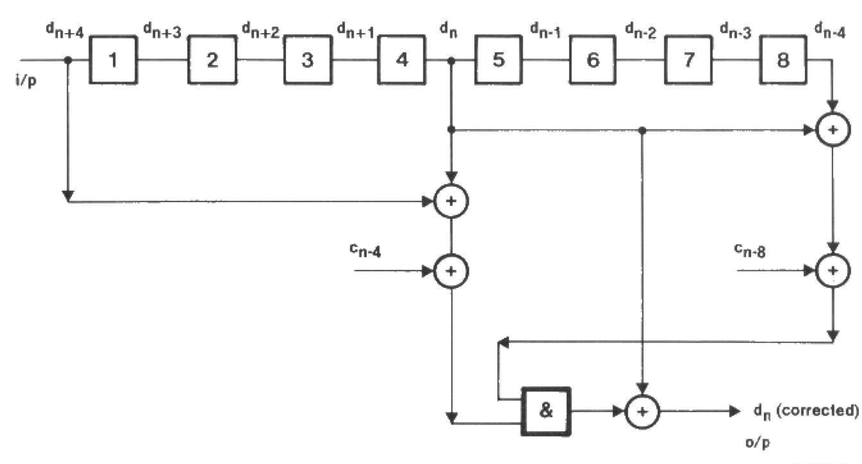


Fig. 2. Decoder for Fig. 1. The output is at bottom right.

data bits. The full transmitted sequence of bits consists of data and check bits in the appropriate order with n=1 in the first position. The decoding operation is in Fig. 2 and requires the two equations

$$c_{n-4}=(d_n+d_{n+4}) \bmod 2 \qquad \text{[Eq. 5]}$$

and

$$c_{n-8}=(d_{n-4}+d_n) \text{ mode } 2. \qquad \text{[Eq. 6]}$$

If the received d_n is incorrect, the output of the AND gate is '1'. The method of correction is simply to add modulo 2 in an XOR logic operation the output of the AND gate to the received d_n. If any of the other four bits are corrupted, the output is '0'. Consequently, the circuit provides only for the correction of d_n provided it alone has been corrupted. For example, if c_{n-8} is also changed, then d_n would not be corrected because the input to the AND gate would change. It should be noted that the calculation of a syndrome as per Section 1 is not required.

Consider the alternative circuit in Fig. 3. This is the method proposed by ETSI for the transmission of data at 1200 bits s^{-1} in the Land Mobile Service. The encoding operation is given by

$$c_n=(d_{n-1}+d_{n-2}) \bmod 2. \qquad \text{[Eq. 7]}$$

The decoding operation, as illustrated in Fig. 4, requires two additional equations:

$$c_{n+1}=(d_n+d_{n-1}) \bmod 2 \qquad \text{[Eq. 8]}$$

and

$$c_{n+2}=(d_{n+1}+d_n) \bmod 2 \qquad \text{[Eq. 9]}$$

to calculate the syndromes. During three successive shifts owing to incoming bits at stages (n+1) and (n+2), the syndromes s_n, s_{n+1} and s_{n+2} are calculated and shifted into the 3-stage shift register on the right. If the received d_n is incorrect, the state of the shift register is (1,1,0) from left to right. The received d_n is used to calculate s_{n+1} and s_{n+2} as per equations [8] and [9], but s_n as per equation [7] should be '0'. To avoid an error in the correction procedure, the next erroneous bit could not occur before d_{n+4}. The bits c_n, d_{n+1}, c_{n+1}, d_{n+2}, c_{n+2}, d_{n+3}, c_{n+3} must be correct to maintain accuracy. Thus the code can only correct one error provided that the following error is at least eight bits later on. In the previous example the syndromes were not required since the check bits preceded the appropriate data bits.

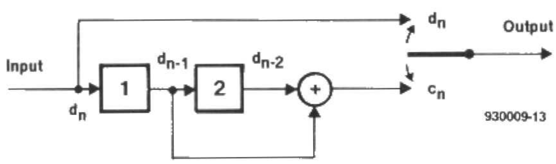


Fig. 3. Convolutional encoder for transmission of data in land mobile services.

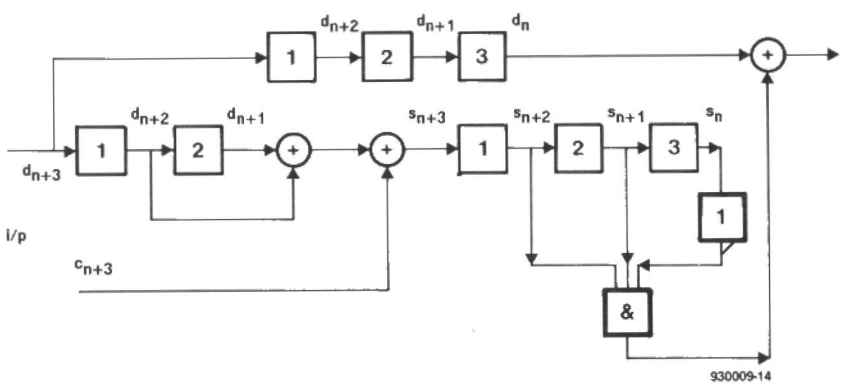


Fig. 4. Decoder for Fig. 3.

Figure 5 shows a convolutional code used by the speech codec in the ETSI specification for Digital Short Range Radio (DSRR). The equations are

$$c_{2n-1}=(d_n+d_{n-3}+d_{n-4}) \bmod 2 \qquad \text{[Eq. 10]}$$

and

$$c_{2n}=(d_n+d_{n-1}+d_{n-3}+d_{n-4}) \bmod 2. \qquad \text{[Eq. 11]}$$

The data bits are not transmitted in their original form as part of the output sequence. If d_n at the input is varied, then part of the output sequence between c_{2n-1} and c_{2n+8} is affected. This is known as the **Constraint Length** and is the length of the output sequence which is affected by the alteration of one bit at the input. This is not a formal definition and different explanations are used in some textbooks.

The ETSI specification does not state a decoding operation which is left to the manufacturer. However, a typical decoder would use

$$d_{n-1}=(c_{2n-1}+c_{2n}) \bmod 2, \qquad \text{[Eq. 12]}$$

but the calculation and interpretation of the syndromes are more complicated. Appendix 2 gives a breakdown for stages 1 to 18. In general terms, to test a value for d_n with complete accuracy, the syndromes corresponding to c_{2n-7} to c_{2n+10} are required. d_n must be the only corrupted bit between d_{n-4} and d_{n+4}. The particular syndromes, which are calculated using the estimated d_n, should be '1' and the other should be '0'. In order to test d_n computed from c_{2n+1} and c_{2n+2} as per Eq. 12, a simple decoder could check the two preceding syndromes s_{2n-1} and s_{2n}. This has the advantage of not needing the calculated values of d_{n+1} to d_{n+4}. The procedure is as follows.

a) d_n is calculated from c_{2n+1} and c_{2n+2} as per Eq. 12.
b) The calculated values of d_n, d_{n-1}, d_{n-3}, d_{n-4} are used to generate new values (estimates) of c_{2n-1} and c_{2n}.
c) The estimated values of c_{2n-1} and c_{2n} from b) are compared with the original received values to deduce the syndromes s_{2n-1} and s_{2n}. If the d_n deduced in a) is erroneous, then both syndromes should be '1' and d_n can be corrected.

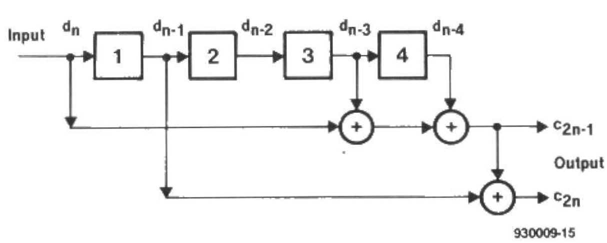


Fig. 5. Convolutional encoder for the DSRR Speech Codec; c_{2n-1} refers to the first and subsequent odd-valued terms; c_{2n} refers to the second and subsequent even-valued terms of the output sequence.

In the actual DSRR standard this convolutional code operates on a block of 43 bits to produce a new block of 86 bits. The reader is referred to the specification for a detailed explanation. The comments after eq. [12] are purely personal and are not in the standard.

The previous nine equations describe the arrangements within shift registers and are written in terms of stages (i.e., time) during their operation. The arrangements can also be expressed as polynomials over GF(2) as

$$g_1(x)=x^4+x^3+1 \quad \text{[Eq. 13]}$$

$$g_2(x)=x^4+x^3+x+1 \quad \text{[Eq. 14]}$$

for the DSRR of Fig. 5. $g_1(x)$ and $g_2(x)$ are known as generator polynomials and the term 'x' represents a shift or delay through one stage of the shift register. This representation is used in the more advanced textbooks.

In general, convolutional codes on their own can be limited, but are usually included with cyclic codes and block permutations to form a hybrid system.

3. BCH codes

A BCH code is a cyclic code with certain mathematical properties to detect multiple errors. Before proceeding further, cyclic codes must be explained in some detail.

A cyclic code is a block code that uses a generator polynomial to produce the check bits. If the block size is n, then code words are written as polynomials over GF(2) (see Appendix 3) as follows:

$$w(x)=[w_n, w_{n-1}, \dots , w_2, w_1]=$$

$$=w_n x^{n-1}+w_{n-1}x^{n-2}+ \dots +w_2 x+w_1. \quad \text{[Eq. 15]}$$

The first r bits, which represent the higher power terms of the polynomial from x^{n-1} to x^{n-1-r}, are the original data bits and the following $(n-r)$ terms are the check bits. The generator polynomial $g(x)$ must be a factor of (x^n+1), that is, $g(x)$ must divide (x^n+1) with no remainder.

Consider an example $g(x)=(x^3+x+1)$ with $n=7$. The procedure to encode the data block [1,1,0,1] is as follows.

a) An estimate of $w(x)$ is taken as $(x^6+x^5+x^3)$ from the data block.
b) $w(x)$ from a) is divided by $g(x)$.
c) The remainder in b) is added back to the estimate in a) to form $w(x)=(x^6+x^5+x^3+1)$ which is the new code word.

Thus, [1,1,0,1] has become [1,1,0,1,0,0,1] with the addition of three check bits into the positions that are low powers of x as per above. It should be noted that $g(x)$ also divides $w(x)$.

At the decoding stage, the received $w(x)$ is validated by computing $w(x)\cdot h(x)$, where $g(x)\cdot h(x)=(x^n+1)$, which is know as the Parity Check Polynomial. Thus, $h(x)$ is the other factor of (x^n+1). The multiplication operation uses $x^n=1$, $x^{n+1}=x$, and so on (see Appendix 5). For the previous example, $h(x)=(x^4+x^2+x+1)$ and $h(x)\cdot w(x)=0$ to indicate that $w(x)$ is correct. If $w(x)$ is corrupted such that (x^6+x^3+1) is received, then the result is $(x^6+x^5+x^2+1)$ and not 0. This is the equivalent of $h(x)\cdot(x^2+x+1)$.

Usually, the method of deduction of a syndrome is to calculate check bits from the received data bits. The generated an d received blocks of check bits undergo an XOR between corresponding bits to produce the syndrome vector. Then, the syndrome is matched in a look-up table for the corresponding error vector and the received data block is corrected. The encoding and decoding operations can also be represented in the form of a matrix where G and H are the generator matrix and parity check matrix respectively. This is only a matter of presentation. The polynominal form has been given here as the matrices were used in Section 1.

In order to detect one error per block, a code must have a **Minimum Distance** of 3 as per Appendix 1. This is the minimum number of variations between two code words. This figure becomes $(2t+1)$ for t errors per block. For a BCH code, the generator polynomial must be primitive (see Appendix 5) and contain $2t$ consecutive roots. For example, if 'a' is a primitive root of (x^n+1), then the generator polynomial must have a, a^2, a^3, ... , a^{2t} as roots. There may be other roots to satisfy the condition that the polynomial is over GF(2) and, consequently, all coefficients must be '0' or '1'. However, the previous condition must be satisfied. Consider the example of $n=15$ as follows:

$$(x^{15}+1)=(x+1)\,(x^2+x+1)\,(x^4+x+1)\,(x^4+x^3+1)\,(x^4+x^3+x^2+x+1). \quad \text{[Eq. 16]}$$

In order to detect and correct three errors per block, the MINIMUM DISTANCE must be 7. Hence, a BCH code must have 6 consecutive powers of a primitive root as roots of its general polynomial. For example,

$$g(x)=(x^2+x+1)\,(x^4+x+1)\,(x^4+x^3+x^2+x+1)$$

or

$$(x^2+x+1)\,(x^4+x^3+1)\,(x^4+x^3+x^2+x+1) \quad \text{[Eq. 17]}$$

would be suitable and would result in a (15,5) code of 5 data and 10 check bits. In Performance Specification MPT 1317, a (63,48) BCH code with generator polynomial $(x^{15}+x^{14}+x^{13}+x^{11}+x^4+x^2+1)$, which is a factor of $(x^{63}+1)$, is used. An additional parity bit is added to produce a (64,48) block code. It has a MINIMUM DISTANCE of 5 and is capable of detecting 4 errors per block or of detecting and correcting 2 errors per block. The reader is referred to the References for further study.

Position

64 63 62 ... 17	16 15 14 ... 2	1
d_{48} d_{47} d_{46} ... d_1	c_{15} c_{14} c_{13} ... c_1	
Data bits	Check bits	Parity bit

Fig. 6. BCH code used for the transmission of data in the Land Mobile Service. The importance of the parity bit is that it detects an odd number of errors.

4. Golay code (23,12)

This is a block code that deserves special mention owing to its unusual properties. The block size is 23, but 12 are data bits. Since this leaves 11 check bits, there is a total of 2^{11}=2048 different error combinations. Hence, the code can, at least in theory, identify up to 2048 possible paterns of error bits. It turns out that it can detect and correct up to 3 errors per block.

There are ${}^{23}C_n=23!/[n!(23-n)]$ possible arrangements of n errors per block. Therefore, for up to 3 errors the number of possible arrangements is

$${}^{23}C_0+{}^{23}C_1+{}^{23}C_2+{}^{23}C_3= 1 + 23+253+1771=2048=2^{11}.$$

Thus, the use of the 11 check bits fits in very nicely with the block size and the general requirements of such a code.

The code is really a cyclic code (see Section 3) with the factors

$$(x^{23}+1)=(x+1)\,(x^{11}+x^{10}+x^6+x^5+x^4+x^2+1)\,(x^{11}+x^9+x^7+x^6+x^5+x+1). \quad [18]$$

Either of the last 2 factors on the right can be used as the generator polynomial. Since there are 12 data bits, this part of the block can be formed by 2 data blocks of 6 bits per block. This permits the use of alphanumeric characters as the data without an awkward division of the individual characters to fit the block size. Unfortunately, the very advantageous properties of this code are unique.

In many applications of the Golay Code systematic decoding is used. This involves the calculation of a syndrome, but is more complicated than the precedures of the previous two sections. The reader is referred to the Reference for further study.

5.Reed-Solomon codes

Reed-Solomon (RS) (n,r) codes are non-binary BCH codes that operate on characters rather than on bits. The 'n' and 'r' refer to the number of characters in the final block and the original number of data characters respectively. If each character is represented by m bits (e.g., ASCII), there is a requirement that $n=2^m-1$. A common value is $m=8$, which gives a block of length $2^8-1=255$ characters. This is quite large as the average computer screen displays 80 characters per line.

If an RS code is required to correct t characters, then $(n-r)=2t$ and the MINIMUM DISTANCE must be $(2t+1)$. For example, $m=3$ and $t=1$ would require $n=7$ and $r=5$. Thus, each block would consist of 7 characters with 2 check characters generated from the other 5.

The procedure for encoding is similar to that in Section 3, but the generator polynomial is formed from $2t$ consecutive powers of a primitive element of GF (2^m) as follows:

$$\prod_{j=1}^{2t}(x-a^j)$$

where 'a' is primitive.

Refer to the example and explanation in Appendix 5. It should be noted that addition and multiplication are in relation to the GF (2^m) and are different from the usual meaning. The reader is referred to the References for a complete mathematical analysis which is not required in this type of overview.

The decoding process requires the calculation of $2t$ syndromes in accordance with the number of check characters. This is followed by a solution of $2t$ simultaneous equations. A number of algorithms have been developed for this purpose. However, there are computational problems for large values of m.

Reed-Solomon (n,r) codes have been implemented on integrated circuits and are used for compact discs.

6. Conclusions

Sections 2 to 5 give an overview of the most common codes. Every method has advantages and limitations which must be weighed according to circumstances. In reality, a system would consist of a hybrid of the various methods such as the procedure in Fig. 7.

INPUT
↓
BCH CODE
↓
PERMUTATION
↓
CONVOLUTIONAL CODE
↓
OUTPUT

Fig.7. Encoding procedure which uses the various methods in cascade.

The purpose of the permutation is to re-order the bits between the two main methods of block and convolutional coding. In many applications it may be omitted. A particular design reflects the requirements and application . Although convolutional codes do not require a block size, they would be operating on a block in a hybrid arrangement in the majority of cases. For example, the DSRR speech codec consists of a BCH code followed by a permutation, a convolutional code operating on a block of fixed length, and a second permutation. This has been discussed in a separate article on DSRR†.

Future developments will probably depend on better methods of implementation. However, a useful point to note is that even if a coding procedure is not capable of correcting a large number of errors, it can still validate data for accuracy. ■

References

1. *The Theory of Information and Coding* by Robert J. McEliece; Addison-Wesley 1977.

2. *An Introduction to Error Correcting Codes* by Shu Lin; Prentice-Hall, 1970.

3. *Information Theory and its Engineering Applications* by D.A. Bell; Pitman, 1968.

4. *Codes and Cryptography* by Dominic Welsh; Oxford University Press, 1988.

5. *A First Course in Coding Theory* by Raymond Hill; Oxford University Press, 1986.

6. *Coding for Digital Recording* by John Watkinson; Focal Press, 1990.

† *Elektor Electronics*, May 1992, p. 46.

Appendix 1: (7,4) Hamming Code

This is a block code that turns 4 data bits into a new block of 7 bits. The positions of the various bits in the new block are:

Position	MSB	7	6	5	4	3	2	1	LSB
Bit		d_7	d_6	d_5	c_4	c_3	c_2	c_1	

The 3 check bits are derived from the 4 data bits by the following equations:

$c_1=(d_3+d_5+d_7)$ mod 2;

$c_2=(d_3+d_6+d_7)$ mod 2;

$c_4=(d_5+d_6+d_7)$ mod 2.

The 3 check bits have $2^3=8$ combinations. Hence, the code can detect one error per block. The set of possible code words is shown in the table in the opposite column.

d_7	d_6	d_5	d_3	d_7	d_6	d_5	c_4	d_3	c_2	c_1
0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	1	1	1
0	0	1	0	0	0	1	1	0	0	1
0	0	1	1	0	0	1	1	1	1	0
0	1	0	0	0	1	0	1	0	1	0
0	1	0	1	0	1	0	1	1	0	1
0	1	1	0	0	1	1	0	0	1	1
0	1	1	1	0	1	1	0	1	0	0
1	0	0	0	1	0	0	1	0	1	1
1	0	0	1	1	0	0	1	1	0	0
1	0	1	0	1	0	1	0	0	1	0
1	0	1	1	1	0	1	0	1	0	1
1	1	0	0	1	1	0	0	0	0	1
1	1	0	1	1	1	0	0	1	1	0
1	1	1	0	1	1	1	1	0	0	0
1	1	1	1	1	1	1	1	1	1	1

There is a minimum difference of 3 bits between any two code words, which is known as the MINIMUM DISTANCE. To detect 2 errors, this distance must be 4 and to correct 2 errors, it is increased to 5 and so on. The procedure to correct an error is:

d_7 incorrect → c_4, c_2, c_1 are not validated
d_6 incorrect → c_4, c_2 are not validated
d_5 incorrect → c_4, c_1 are not validated
d_3 incorrect → c_2, c_1 are not validated

The sum of the indices of the check bits that are not validated gives the location of the error.

Appendix 2: Convolutional code for the DSRR Speech Codec

n	Transmitter	Receiver	
	$c_1=d_1$		s_1
1	$c_2=d_1$	'0'	s_2
	$c_3=d_2$		s_3
2	$c_4=d_2+d_1$	d_1	s_4
	$c_5=d_3$		s_5
3	$c_6=d_3+d_2$	d_2	s_6
	$c_7=d_4+d_1$		s_7
4	$c_8=d_4+d_3+d_1$	d_3	s_8
	$c_9=d_5+d_2+d_1$		s_9
5	$c_{10}=d_5+d_4+d_2+d_1$	d_4	s_{10}
	$c_{11}=d_6+d_3+d_2$		s_{11}
6	$c_{12}=d_6+d_5+d_3+d_2$	d_5	s_{12}
	$c_{13}=d_7+d_4+d_3$		s_{13}
7	$c_{14}=d_7+d_6+d_4+d_3$	d_6	s_{14}
	$c_{15}=d_8+d_5+d_4$		s_{15}
8	$c_{16}=d_8+d_7+d_5+d_4$	d_7	s_{16}
	$c_{17}=d_9+d_6+d_5$		s_{17}
9	$c_{18}=d_9+d_8+d_6+d_5$	d_8	s_{18}

The left and right sides show the encoding and decoding operations respectively. Consider the required procedure to test the calculated d_5, computed at the receiver from c_{11} and c_{12}, for possible correction. This value must be used to calculate s_9, s_{10}, s_{15}, s_{16}, s_{17}, and s_{18} as indicated. If d_5 is the only incorrect value owing to an error in c_{11} or c_{12}, then these syndromes should be '1' and the other syndromes '0'. In a simple decoder, s_9 and s_{10} could be used, which would avoid the successive terms d_6, d_7, d_8 computed after d_5.

Appendix 3: Polynomials over GF(2)

Consider the following two polynomials

$$f_1(x)=x^3+x^2+1$$
$$f_2(x)=x^2+x+1.$$

The coefficients of the various powers of x are all '0' or '1'. The various operations do not change, b ut the individual terms must be added m odulo 2. For example, the product of the two polynomials,

$$f_1(x)\cdot f_2(x)=x^5+x+1,$$

has degree 5, but the terms x^4, x^3, and x^2, which would result in a multiplication in the usual manner, are not present. This is because $x^4+x^4=0$, since 1+1=0 mod 2. The same cancellation occurs for x^3 and x^2. In the article all polynomials are of this form.

An irreducible polynomial over GF(2) is one that cannot be factored such that the factors are also polynomials over GF(2). For example, (x^2+x+1) is irreducible, but (x^2+1) is reducible. Since (x^2+1) equals $(x+1)^2$ over GF(2), $(x+1)$ is a factor of (x^2+1).

Appendix 4: Galois Fields

The expression GF(2) means a field of 2 elements (0 and 1) and the arithmetic operations of addition and multiplication are modulo 2. The term field has a very precise mathematical meaning. A set $A=\{a_n, a_{n-1}, \ldots, a_2, a_1\}$ is a group under the operation '·' if it satisfies the following four properties.

1) **Closure** $(a_i \cdot a_j)$ is also in A for all i and j.
2) **Associative Law** $(a_i \cdot a_j)\cdot a_k=a_i\cdot(a_j\cdot a_k)$ for all i, j, k.
3) **Identity** $a_i\cdot e=a_i$ for all i for a particular element 'e' in A.
4) **Inverse** $a_i\cdot a_i^{-1}=e$ for all i. Every element has an inverse that is also in A. For example, e is zero or one for addition or multiplication respectively.
5) If $a_i\cdot a_j=a_j\cdot a_i$ for all i and j, the set is a commutative group.

The set of integers modulo n: $\{0, 1, 2, 3, \ldots, (n-1)\}$ is a group under addition. This is obvious and does not require proof. It is also a group under multiplication, but n must then be prime. If, in order to satisfy the CLOSURE property, $n=a\cdot b$, where a and b are integers smaller than n, $a\cdot b=0$ means that $a=0$ or $b=0$. Hence, n must have no factors and must be prime. For example, take $n=17$. The arithmetic is modulo 17 and all integers must be 0, 1, 2, ..., 16. The first two properties are obvious and IDENTITY $e=1$. Thus, the only outstanding property is the INVERSE. If $a=19$, there must be an element such that $a\cdot b=1$ mod 17. If $b=2$, $a\cdot b=18$, which gives a remainder and is the IDENTITY, on division by 17. Consequently, 2 is the multiplicative inverse of 9 for a multiplication operation mod 17. Similarly, 13 would be the inverse for 4, since 13×4=52 and the remainder on division by 17 is 1. Every element has an inverse within the set. Hence, it is a group un der multiplication.

A field is a commutative group under addition and under multiplication. GF(2) has just 2 elements, but satisfies all the conditions. The arithmetic operations are modulo 2. It is a finite field in that it has a finite number of elements. Every finite field is of the form GF(p^m) where p is a prime and m is a positive integer. This point need not be considered further for this type of article.

Appendix 5: Cyclic Groups

A cyclic group is one that has a generator element as follows: $\{a, a^2, a^3, \ldots, a^{n-1}\}$ where $a^n=e=a^0$. Consider the following set of eight elements

$a^0=(0,0,0)$
$a^1=(0,0,1)$
$a^2=(0,1,0)$
$a^3=(0,1,1)$
$a^4=(1,0,0)$
$a^5=(1,0,1)$
$a^6=(1,1,0)$
$a^7=(1,1,1,)$.

$$\to a \to a^2 \to a^3 \to a^4 \to a^5 \to a^6 \to a^7 \to a^0 \to$$

If the operation '·' is defined in the usual manner with $a^i\cdot a^j=a^{i+j}$, the set is a cyclic group with a^1 as the generator.

$$a^2\cdot a^3=(0,1,0)\cdot(0,1,1)=a^5=(1,0,1)$$

as per the table. Terms such as $a^8=a^0$ and $a^9=a^1$ and so on. In electronic form, the operation '·' as defined is the equivalent of addition with carry up to but not including the MSB.

The equation $x^n+1=0$ has n roots that form a cyclic group of order n and can be represented as in the example. It must be emphasized that a^2 is not necessarily 'a squared' in the usual sense. A primitive root (e.g., a^m) is a generator for the full group: a^m, $(a^m)^2$, $(a^m)^3$ and so on with no missing terms. The sequence does not repeat until n stages has been reached. For a non-primitive root, this is not the case.

A primitive polynomial has a primitive root (or roots) as defined above. The polynomial is over GF(2) as per Appendix 3, but the root(s) is usually complex.

READERS' LETTERS

ARE DESIGNERS GETTING STALE?

Dear Editor—Many electronics magazines have a tendency to repeat constructional projects over the years. *Elektor Electronics* is not too bad, but I have noticed that some other magazines continually repeat certain projects. It is as though they are stuck for new ideas, and yet there are many projects that I have never seen in an electronics construction magazine. Two examples: an audio pick-up probe with increased sensitivity and a progressive wire locator system. Although both devices are common in the USA*, they are not available here in the UK and would, therefore, lend themselves to a future constuction project.

P. Male, Pershore

*Available from Time Motion Tools, 12778 Brookprinter Place, Poway, CA 92064, USA, Telephone (619) 689 7272.

Your letter has been copied to our Head of Design, as well as to several of our American free-lance contributors. Note, in passing, that we have published one or two wire locators over the years, which have proved very popular. However, these used components that are now out of date, so replacements based on modern components would be no luxury. Editor

THANKS!

Dear Editor—I would like to put on record my sincere thanks for the help received as a direct result of your including my cry for help in repairing my Freeway phone (Letters, November 1992). I especially appreciated the speed with which you phoned through details of the other readers who were offering assistance. The phone is now working again! I would also add that your magazine was the only one of three which I contacted that was prepared to assist.

I.M. Tasker, Grantham.

I am pleased to read that your troubles have been resolved with our assistance. One of our aims is to help readers in trouble: we don't always succeed, but we always try. Editor

AM BROADCAST RECEIVER

(October 1991)

Dear Editor—I am attempting to construct the 'AM Broadcast Receiver', but I am having difficulty with the PLL section. This is because on the circuit the marked pin connections of IC_4 do not appear to be correct.

S. Farrant, Yangebup, Western Australia

The 'pin numbers' of the 4053 in the PLL are not incorrect: they are not pin numbers but pin function indications. What you may have read as '10' and '11', are acutally '10' and '11', that is, 'input nought' and 'input one', respectively. Other readers may also note that in our circuit diagrams pin numbers are always printed outside the IC and pin functions inside.

The 4053 contains three identical change-over switches with a common inhibit control. The reason that we have not given pin numbers in this particular case is that there is no corresponding PCB design. Constructors are, therefore, free to choose tjeir own switches (a, b, and c), which are identical. Editor

PHONE/FAX INTERFACE

Dear Editor—I have come quite frequently across people who would like to use their internal fax modem in a single line mode and thus require a phone/fax interface with the ability to handle an answering machine. Additionally, it would be useful to provide some ideas of how to protect your phone line from lightning strikes effectively and reduce line noise at the same time. Some of the input circuits of the inexpensive modems are rather flimsy in this regard. Here in Florida this is an ongoing problem and I am sure there is a requirement for such protection in other parts of the world. Do you have an expert on phone line interface circuits who could either design such a phone/fax interface or do you

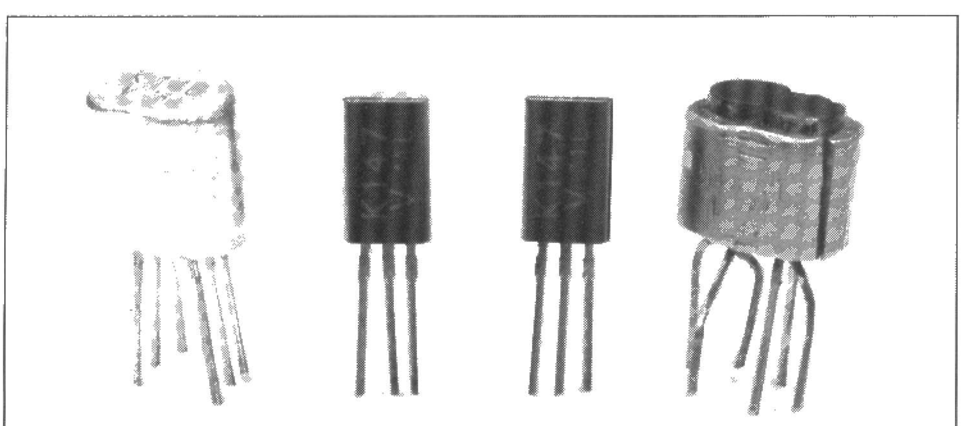
CORRECTIONS AND UPDATES

LFA150-A Class-A amplifier

November and December 1991

Replacement for 2SK146V.

We have recently been informed by Toshiba that the dual FET Type 2SK146V used in the LFA150-A design is no longer manufactured. The 2SK146V is not a dual FET in the true sense of the word, i.e., there are no two FETs on a single chip. Rather, it consists of two FETs, each in its own enclosure, which are held together by a metal ring. Such a construction is readily reproduced by clamping two 2SK147V FETs together, using a small piece of metal (e.g., copper or brass).



The photograph illustrates the construction of the replacement dual FET. In practice, the 'imitation' works perfectly. Note, however, that the pin connections of the replacement FET are different from the original 2SK146, which has facing identical pins. By contrast, the dual 2SK147V construction has identical pins in mirrored positions. Fortunately, this is simple to resolve by bending the outer pins (drain and source) of one FET such that the pin positions are swapped. (920163)

Sound sampler for Amiga

November ~~1991~~. 1992

Capacitor C9 is mising from the parts list and the circuit diagram. C9 is a 100-nF decoupling capacitor fitted near IC7 (see component overlay).

LEDs D2 and D4 should be transposed, both in the circuit diagram and the parts list. D2 is the ERROR LED, and D4 the LEFT LED. (920074)

NOTE? ADDED TO NOV 1992 P 56

have an idea where I could obtain literature describing the same?

Jurgen Kruppa, Delray Beach, Florida

Regrettably, we have no phone line expert on our staff, but trust that interested expert readers will come forward with ideas. In the mean time, we have approached various telecoms operators for suitable literature and as soon as this to hand, we will pass it on to you. Editor

COMPONENT RATINGS

In resistor and capacitor values, decimal points and large numbers of zeros are avoided wherever possible. Small and large values are usually abbreviated as follows:

p (pico-) $= 10^{-12}$
n (nano-) $= 10^{-9}$
μ (micro-) $= 10^{-6}$
m (milli-) $= 10^{-3}$
k (kilo-) $= 10^{3}$
M (mega-) $= 10^{6}$
G (giga-) $= 10^{9}$

Note that nano-farad (nF) is the international way of writing 1000 pF or 0.001 μF. Resistors are $^1/_3$ watt, 5% metal film types unless otherwise specified.

The direct working voltage of capacitors (other than electrolytic or tantalum types) is assumed to be ≥60 V. As a rule of thumb, a safe value is about 2× direct supply voltage.

Direct test voltages are measured with a 20 kΩ/V meter unless otherwise specified.

Mains (power line) voltages are not listed in the articles. It is assumed that our readers know what voltage is standard in their part of the world.

Readers in countries that use 60 Hz supplies, should note that our circuits are usually designed for 50 Hz. This will not normally cause problems, although if the mains frequency is used for synchronization, some modification may be required.

The international letter symbol '*U*' is used for voltage instead of the ambiguous '*V*'. The letter V is reserved for 'volts'.

The size of a metric bolt or screw is defined by the letter M followed by a number corresponding to the overall diameter of the thread in mm, the × sign and the length of the bolt or screw, also in mm. For instance, an M4×6 bolt has a thread diameter of 4 mm and a length of 6 mm. The overall diameter of the thread in the BA sizes is: 0 BA = 6.12 mm; 2 BA = 4.78 mm; 4 BA = 3.68 mm; 6 BA = 2.85 mm; 8 BA = 2.25 mm.

SWITCHBOARD

Switchboard allows all PRIVATE READERS of *Elektor Electronics* one FREE advertisement of up to 108 characters, including spaces, commas, numerals, etc., per month.

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FOR SALE. Maplin Z80 computer incl. power supply, keyboard, PC assembler and various bits and bobs. £70 (shareware assembler). Please write or phone to Jonathan Miller, 16 Prince Rupert Road, Worcester WR5 1AF. Telephone (0905) 358 742.

WANTED. Flex (6809) hardware/software. Please phone Phil on 081 898 8763.

WANTED. *Time Bases* by O.S. Puckle. Published 1941/42 in association with A.C. Cossor Ltd. Please write or phone to Albert B. Petrie, 54 Clober Road, Milngavie, Glasgow G62 7SR; Telephone 041 956 1041.

FOR SALE. Two DX553 PA valves, £50. 2m PA 2×4C×350 and PSU bits, £250 o.n.o. Phone Andy on (0535) 652 512.

FOR SALE. Link 110 3-tube colour studio camera, incl. lens, tripod, manuals, VGC. £300 o.n.o. Phone Matt on (0636) 821 953 (eves).

WANTED. SPO256-AL2 speech chip. Please write or phone Brian Busuttil, 370 Ghar Id-Dud Street, Sliema, Malta; Phone 334 150.

FOR SALE. BBC Master 128 and Cuman twin DS 40/80T drives. Sensible offers to Mr S. Gojke, 7 Lewes Gardens, Whitleigh, Plymouth, Devon PL5 4EB.

FOR SALE. Gould OS3000, 40 MHz dual trace scope, £90. 1.2 metre glas-fibre dish tripod AZ/EL adj 1700 MHz feed, £60. Phone Mr C. Scrase on (0884) 32388.

FOR SALE. Blackstar 600 frequency meter, NiCds plus ant., £90. RS 50 Ω dummy loads. 200 W, £85; 15 W, £8. All as new. Phone Mr. R. Jackson on (0602) 462 189.

WANTED. Chip for Kenwood car amp. Toshiba make TA7250BP (?). Please write to Mr S. Mercer, 16 Manor Farm Rise, North Leverton, Retford, Notts DN22 0BH.

FOR SALE. CMOS RAMs 6264, £0·80; 62256, £1·90; 6IC67, £0·80; 256 k × 4-bit DRAM, £2. Phone Jim on (0252) 518 538.

FOR SALE. Portable alarm, 9 V, 120 dB loud siren. Write to Shih Chi Kuang, 118 Bedok North St. 2, # 04-190, Singapore 1646.

HELP. Where can I buy the Spoerle slider switches for the Elektor RS232 tester (July 1992). Call Jim on (0624) 824 380.

Send this coupon to
Elektor Electronics (Publishing)
P.O. Box 1414
Dorchester DT2 8YH
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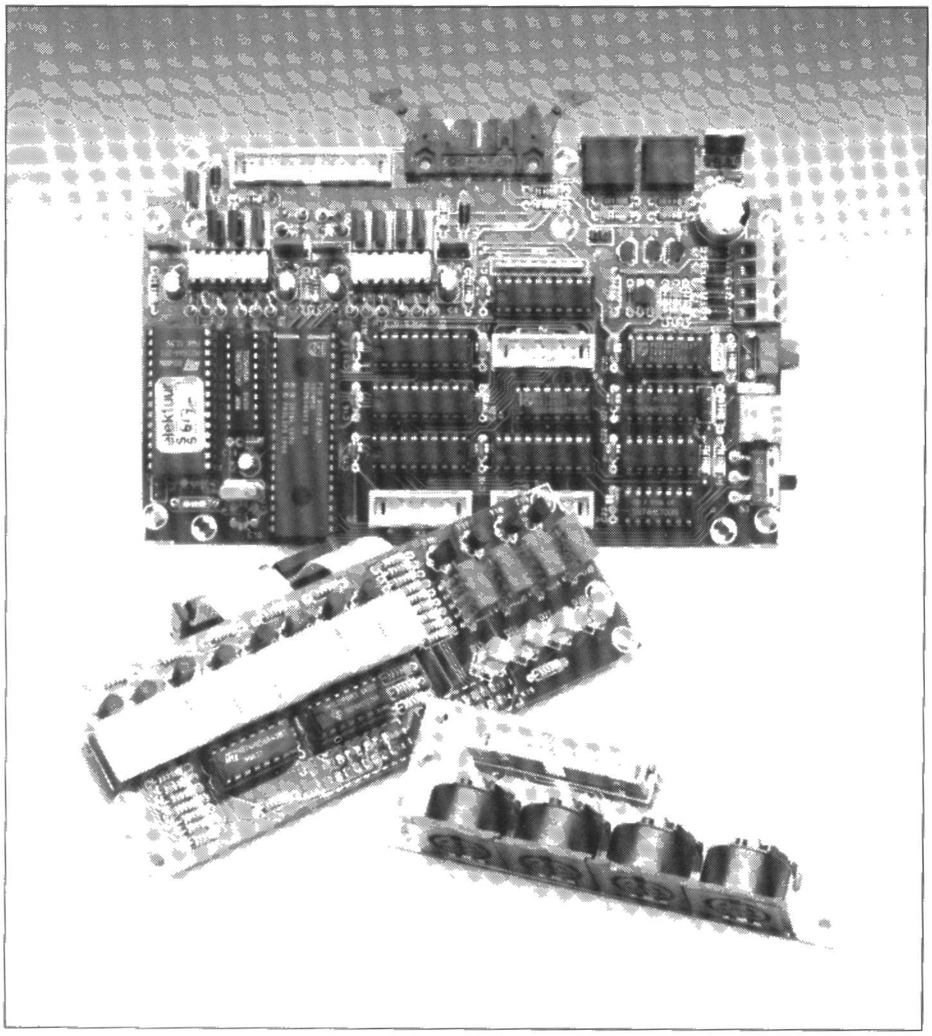
Block capitals please – one character to each box

ELEKTOR ELECTRONICS 01/93

Name and address MUST be given

DIGITAL AUDIO/VISUAL SYSTEM

PART 3: MAIN UNIT



In the first two parts of this article we concentrated mainly on the system outline and the dissolve unit. This time, we tackle the construction of the main unit, which forms the central control of the DiAV system. As promised, we will also show you how all modules can be fitted into a single enclosure.

Design by A. Rietjens

Correction to Part 2:
The parts list on page 22 of the December 1992 issue states that self-adhesive foil number 920022-2 is the rear panel foil for the dissolve unit. This is incorrect: self-adhesive foil number 920022-1 consists of the front panel foil and the rear panel foil, which must be separated by cutting. The layouts are shown in Fig. 21. The foil with order code 920022-2 is for the infra-red remote control transmitter, which will be discussed in Part 4.

After reading last month's instalment, you may be wondering what to do with the two left over printed circuit boards. Well, these are used in the main unit to enable the connections to the 'printer' and the timecode interface to be made in a way similar to connector K2. More about this further on.

The construction and test of the main unit concentrate mainly on the Z80 card, the software for which will be discussed in next month's (final) instalment. For those of you who have not yet built the Z80 card, now is a good time to do so. Do not, however, fit the ICs as yet. You will also need to build the RC-5 infra-red receiver and the mini keyboard for Z80 (*Elektor Electronics* December 1992). The corresponding articles will provide you with all the necessary construction details — for references, see Part 1 of this article. The PCB for the mini keyboard needs to be modified: cut off the side pieces with the additional fixing holes. This is necessary to enable the PCB to be fitted into the main unit enclosure. Although the infra-red control system gives complete control over the functions of the DiAV main unit, a PC-XT keyboard may still be useful if you want to enter a control sequence for a long series of slides. To be able to make the best possible use of the infra-red control, fit the 'repeat' jumper, JP1, and short-circuit diode D4. This enables the Z80 card to detect that a key is held depressed, whereupon appropriate action is taken.

The construction of the main unit is thus limited to cutting and drilling the metal enclosure. Since there are quite a few holes, this may take some time. The fitting of the Z80 card in the Retex RE.4 enclosure is detailed in the relevant article. When the Z80 card is used in the main unit described here, the printer connector, K9, is omitted and replaced by the dissolve unit connection on K9'. Do **not** solder a connector in position K9 to prevent errors when the unit is wired. The connections to the outside world are made via a 14-way flatcable connector, a 14-way flatcable connector for PCB mounting, and a 14-way header with eject handles (side latches), which is mounted on adaptor board K16/K17.

The EXT1 and EXT2 outlets are brought out in a similar manner with the aid of connector board K14/K15. One of these connections is used later to hook up the timecode interface. The software has a routine that looks for the connector to which the interface is actually linked. The advantages of this will become evident when we describe the 'compact' version of the DiAV system.

Now, if you feel a little confused about which connections to make and not to make, have a look at Fig. 27, which shows a complete overview of the interconnections between the various modules that make up the DIAV main unit.

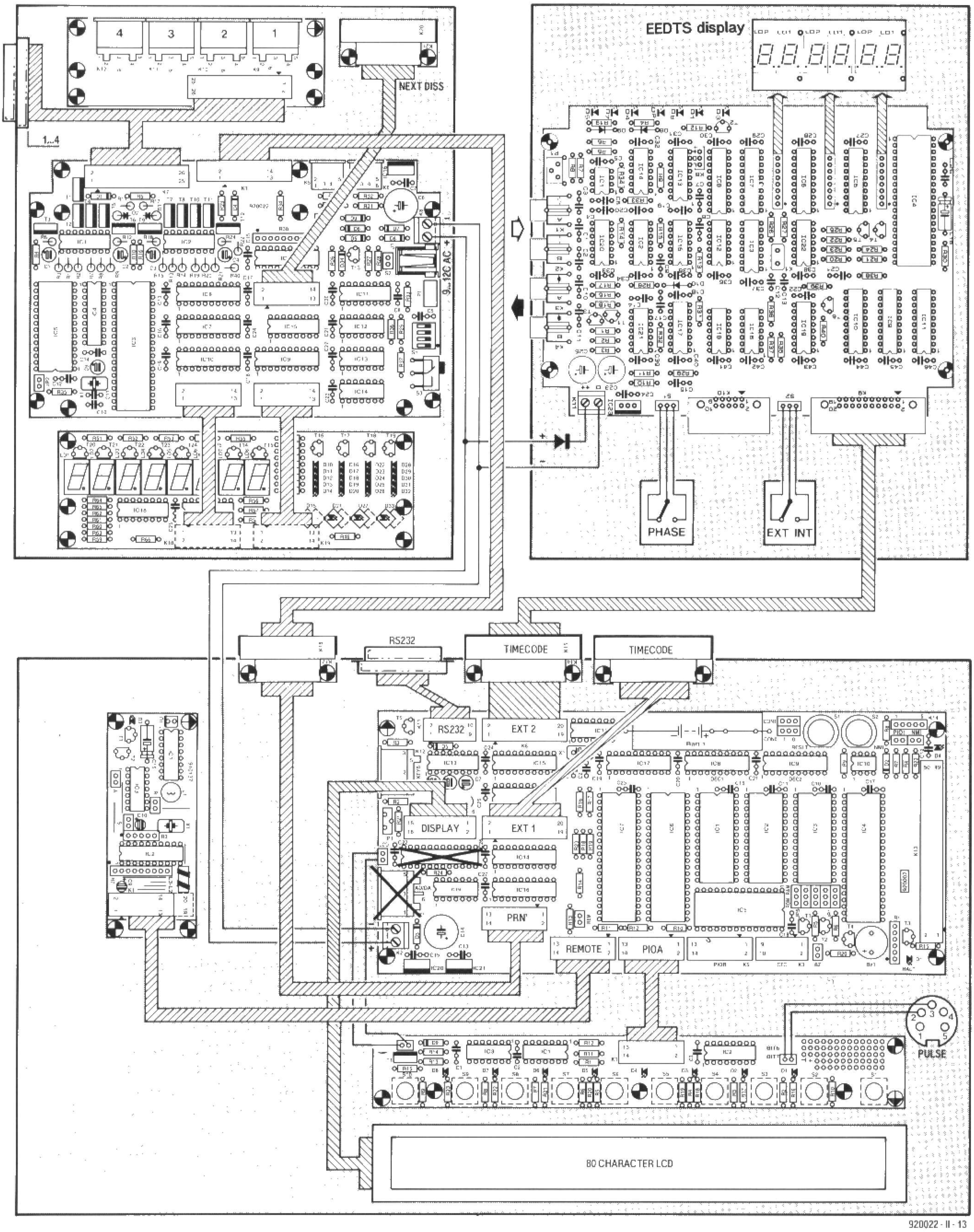


Fig. 27. This overview shows how the various modules that make up the DiAV system are interconnected. If everything is built into a single enclosure, the connector boards with K14-K17 on them, and the LED displays, are omitted.

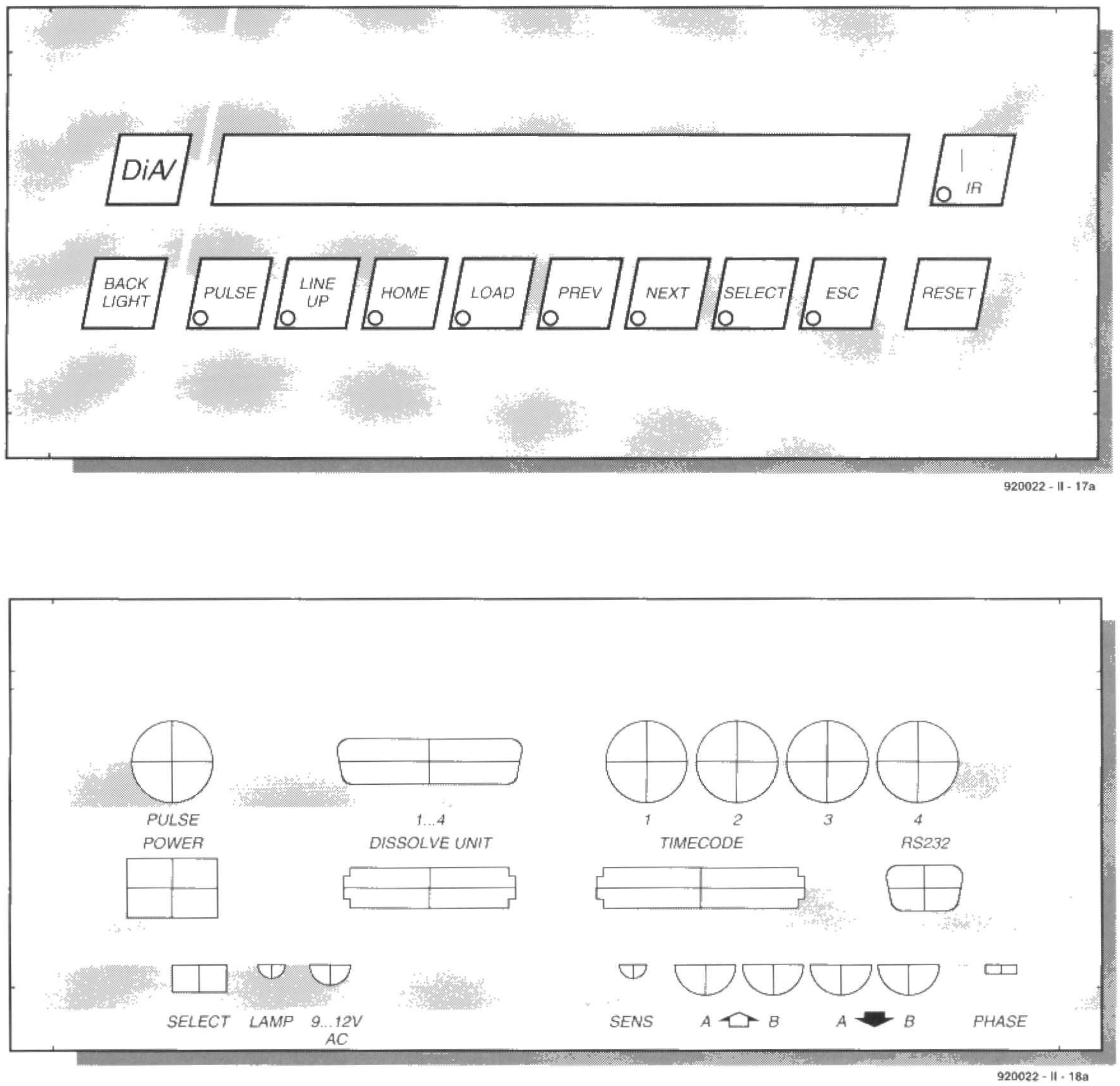


Fig. 28. These two self-adhesive foils (front and rear panel) are available ready-made through our Readers Services. They can be cut to size to fit on three different enclosures, as indicated by the small marks at the sides. The keytop areas are flexible enough for the keys to be operated reliably.

A stylish front panel foil has been designed for the DiAV main unit. This comes together with a rear panel foil, and can be ordered as item 920022-F3 through our Readers Services. The foils (Fig. 28) are supplied with 1:1 drilling templates (Fig. 29). Their dimensions are such that they can be used on three different types of Retex enclosure: the RE.4, R0.82 and R0.103. Depending on the enclosure used, you may have to reduce the width of the front panel foil a little (see Fig. 29). If you use the RE.4 enclosure, make sure to mark the short side first with a pencil, since this mark is lost when the long side is reduced.

It will be noted that the front panel material is flexible enough to allow you to operate the push-buttons behind it, provided the cut-outs are made exactly as indicated by the drilling template. The holes for the switches are drilled with a 12 mm drill. Use the drilling template and a centre punch to mark the locations of the switch corners (see Fig. 31), and a small file to make the actual 'corners'.

The keyboard PCB is mounted such that the keytops protrude a little from the aluminium surface. The LEDs must, however, not protrude, and are best soldered after the keyboard has been mounted at the right distance from the front panel. Since it is necessary to accurately adjust this distance (smaller than 5 mm), it is best to use stiff springs as PCB spacers.

Power supply

If all modules are fitted in separate enclosures, two mains adaptors suffice to power the control system: one 1-A mains adaptor with a.c. output for the dissolve unit, and one with 1-A d.c. output for the main unit and the timecode interface (the latter is then powered via the flatcable connection).

In this configuration, it is best to use a jack connector with a thin centre pin, plus an associated plug. For the main unit, use a similar connector, but one with a thick centre pin. The thing about this arrangement is that it prevents the a.c. adaptor being connected to the main unit. Do not use audio 'jack' connectors and plugs for the power supply, since these are prone to causing short-circuits when the plug is inserted or removed. If you can not get hold of an adaptor with a.c. output, use a d.c. type instead from which the rectifier diodes and the smoothing capacitor(s) have been removed (provided you can open the

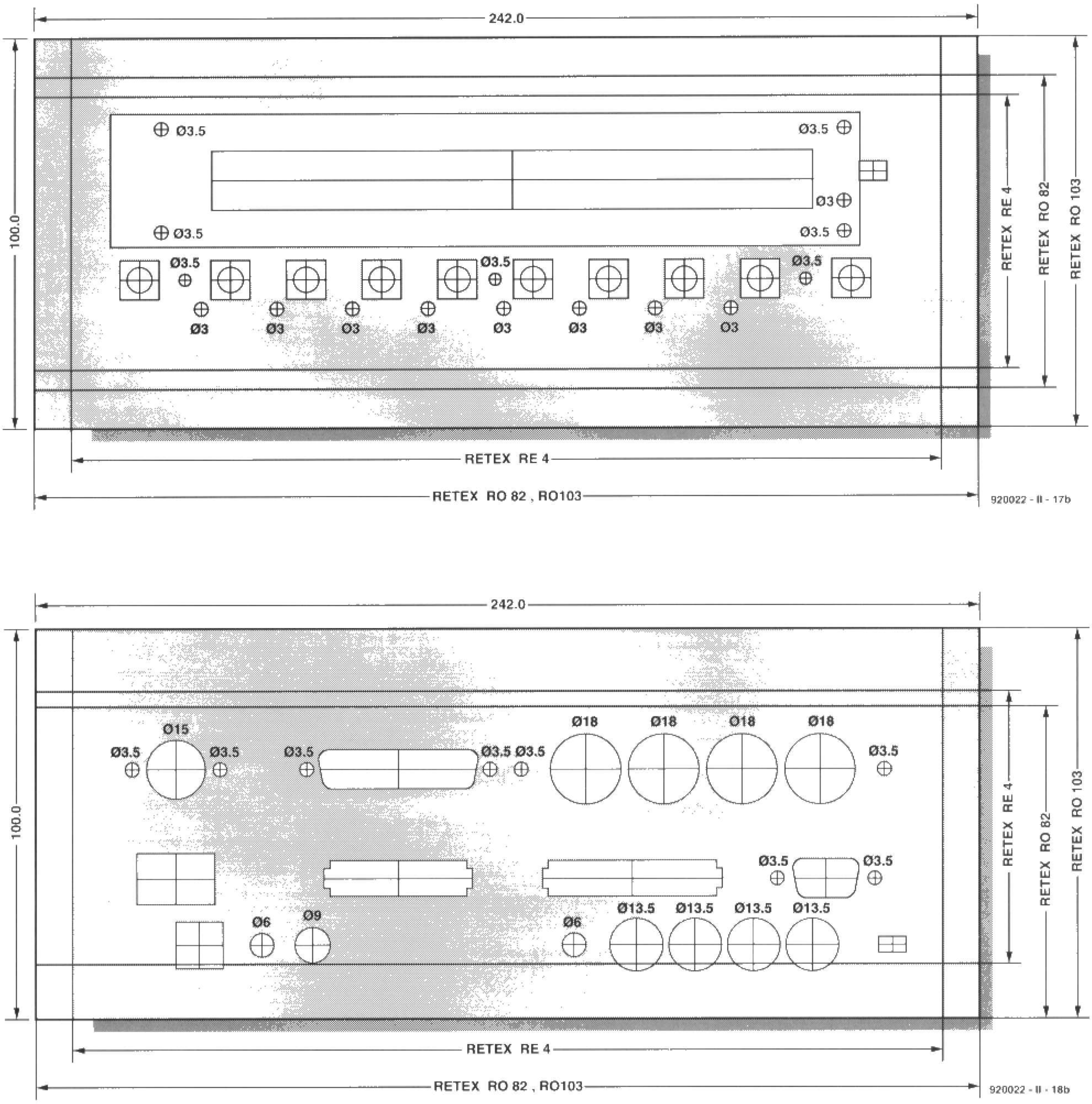


Fig. 29. These drilling templates, of which 1:1 copies are supplied with the front and rear panel foil combination, should help you to produce accurately drilled and filed front and rear panels for the DiAV main unit.

adaptor). The output wire of the modified adaptor is connected to the a.c. side of the diode bridge in the adaptor.

Everything in one enclosure

As already mentioned, it is possible to fit the timecode interface, the dissolve unit and the main unit into a single enclosure. In this way, a compact control unit is obtained that is easily carried about. This will be particularly valued if you are frequently out and about with your equipment, doing slide shows. The enclosure chosen is a pretty solid, all-aluminium, type. Its one disadvantage with respect to the RE.4 enclosure is that it is a little more difficult to cut and drill, the reason being that the aluminium is thicker. The 'three-in-one' construction is cheaper than using separate enclosures to house the modules, since the displays and the additional enclosures need not be purchased. On the down side, you forfeit the 'large distance' LED displays on the dissolve unit and the timecode interface. This disadvantage plays a role mainly when the timecode unit is programmed. Although all functions are indicated on the LC display, it can not be denied that this is more difficult to read than the set of LED displays. Well, the choice is yours!

The main unit front panel foil is designed such that it fits both on the Retex R0.82 and the R0.103 enclosure. These enclosures are virtually identical, with the exception of their height: 8 cm and 10 cm respectively. The R0.82 allows the most compact construction, but unfortunately is not a stock type (supply time approx. 3 months). By contrast, the R0.103 is available from stock. Hence, those of you who insist on building as compact a unit as possible will have to be patient with the Retex supplier.

The prototype of the DiAV main unit

COMPONENTS LIST

Components list for the DiAV main unit:

All components for the 'mini keyboard for Z80' (December 1992).

All components for the Multi-purpose Z80 card (May and June 1992), including the infra-red receiver and transmitter, however excluding the following components and software:
IC1 (Z80 BIOS); IC2 (RAM or EPROM); IC8 and IC9 (Z80 BIOS GALs); IC11 (AD7569 ADC/DAC); C14 (220µF/16V); D2 (BAT85); K1 (6-pin 240° DIN socket); K9 (PRN connector); the 15-way sub-D connector; the diskette with the Z80 BIOS (ESS 1711); (optionally) the PC-XT keyboard.

The following components are added:
C14 = 1000µF 16V
D2 = BAS45
IC2 = 43256 (32 kByte static RAM)
K17 = 14-way PCB mount flatcable connector
K16 = 14-way PCB header with side latches (to dissolve unit)
20-way flatcable connector
K14 = 20-way PCB mount flatcable connector
K15 = 20-way PCB header with side latches (to dissolve unit)

Front panel foil for IR remote control transmitter (920022-F2; see page 70)
Front & rear panel foil for main unit (920022-F3; see page 70)

Components list for 'all in one' (compact) construction:

All components for the main unit

All components for the dissolve unit, except:
S3; K1; K5; K6; K20 and the components for the display section. Use a 14-way box header for K1, and a 14-way straight header with side latches for K20.

All components for the timecode interface, except K9 and the display. K9 is change into a 20-way box header.

Enclosure: Retex* R0.82 (h = 8cm) or R0.103 (h = 10cm)

* Retex, Jerusalén 10, 08902 Hospitalet, Barcelona, Spain. Tel. +34 3 335 5562. Fax: +34 3 335 7468.
Distributors:
Boss Industrial Mouldings Ltd., James Carter Road, Mildenhall, Suffolk IP28 7BD. Tel. (0638) 716101.
C-I Electronics, P.O. Box 22089, NL-6360 AB, Nuth, Holland. Fax: +31 45 241877.

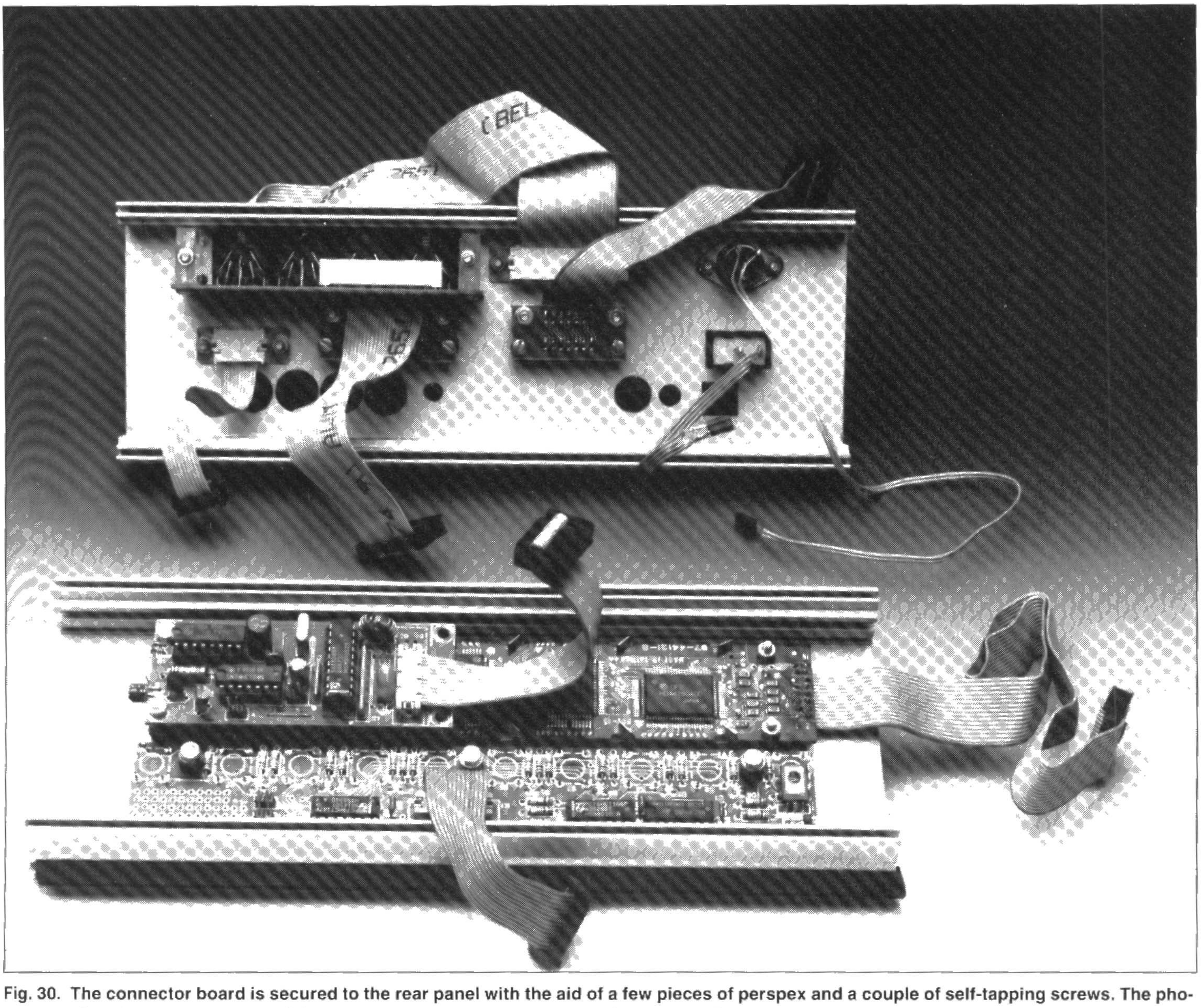


Fig. 30. The connector board is secured to the rear panel with the aid of a few pieces of perspex and a couple of self-tapping screws. The photograph also shows how the remaining components are mounted on to the two panels.

was built into a R0.82 case. If you use this also, be sure to mount the ICs on the mini keyboard PCB directly on to the board, i.e., without IC sockets. If you do not, you will not have enough room to fit the other modules in the case.

The Retex enclosures consist of two identical panels (front and rear), which are secured to one another by two side panels (see the photographs). Apart from the guide slots for the top and the bottom cover, the front and rear panels also have a kind of rails in which bolts and nuts may be mounted. We used this possibility to fit the bottom plate (1.5 mm thick), on top of which the dissolve unit PCB and the timecode PCB may be mounted (using 5-mm high PCB pillars and screws with countersunk heads). A second base plate is mounted above these PCBs, using PCB pillars with a length of at least 35 mm. This plate serves to mount the Z80 card. The dimensions of the two plates (Fig. 32) are such that the bottom plate can be slid into the enclosure from one side, along its rails, with the two Pcbs on it, and all parts fitted on to the front and rear panel. When the smaller case is used, countersunk M4 screws must be used at the side of the display.

Since the LED display of the dissolve unit is omitted when everything is built into a single case, it is difficult to see whether or not the circuit is 'alive'. To have an indication that it all works, connect a LED in series with a 220-Ω resistor to pins 10 (anode) and 15 (cathode) of IC10. This LED takes over the function of the decimal point on the LED display, and will flash if no alternating voltage is applied. In all other cases, it will light normally.

The Z80 card is mounted on a small plate, which is also used to secure the two voltage regulators (see Fig. 33b). First mount the regulators on to the plate, and do not solder them to the card before this has been secured in its final position. Alternatively, make a connector from two pieces of IC socket as illustrated in Fig. 33c. Remember, however, that such a connection is not meant to be broken often. The PCB pillars may be glued on to the mounting plate, which then forms one assembly with the Z80 card.

After sliding the bottom plate into position, make all the connections to the PCBs fitted on it (Fig. 33d). Next, mount the Z80 card plus mounting plate, and connect its wiring (Fig. 33e).

As you are working on the wiring, you wonder about the best way to connect the power wires to the modules. The simplest way to do this is to power all board from the dissolve unit. This means that PCB terminal block K8 must be mounted with its wire entry side pointing to the inside, i.e., not to the board edge as usual. The connecting wires may then be fed in from the inside. Remember, K8 carries the rectified voltage of the a.c. adaptor. This may **not** be smoothed, hence the extra diode in the power supply line to the timecode interface (do not forget to put switch S2 on the timecode interface to position B-C). The Z80 card has a polarity reversal protection in the form of diode D3, so that the raw direct voltage is retained. Capacitor C14 must have a minimum capacitance of 1000 µF, and a minimum working voltage of 16 V. A

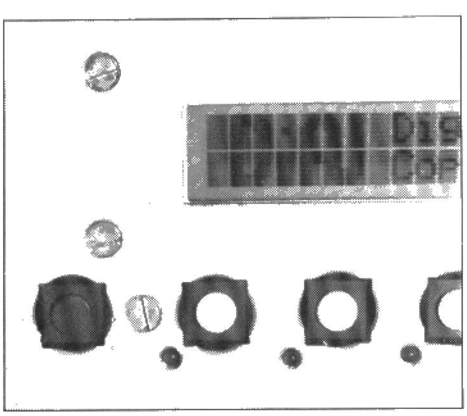


Fig. 31. Drill 12-mm dia. holes for the switches, and file the corners to allow the switches to protrude slightly.

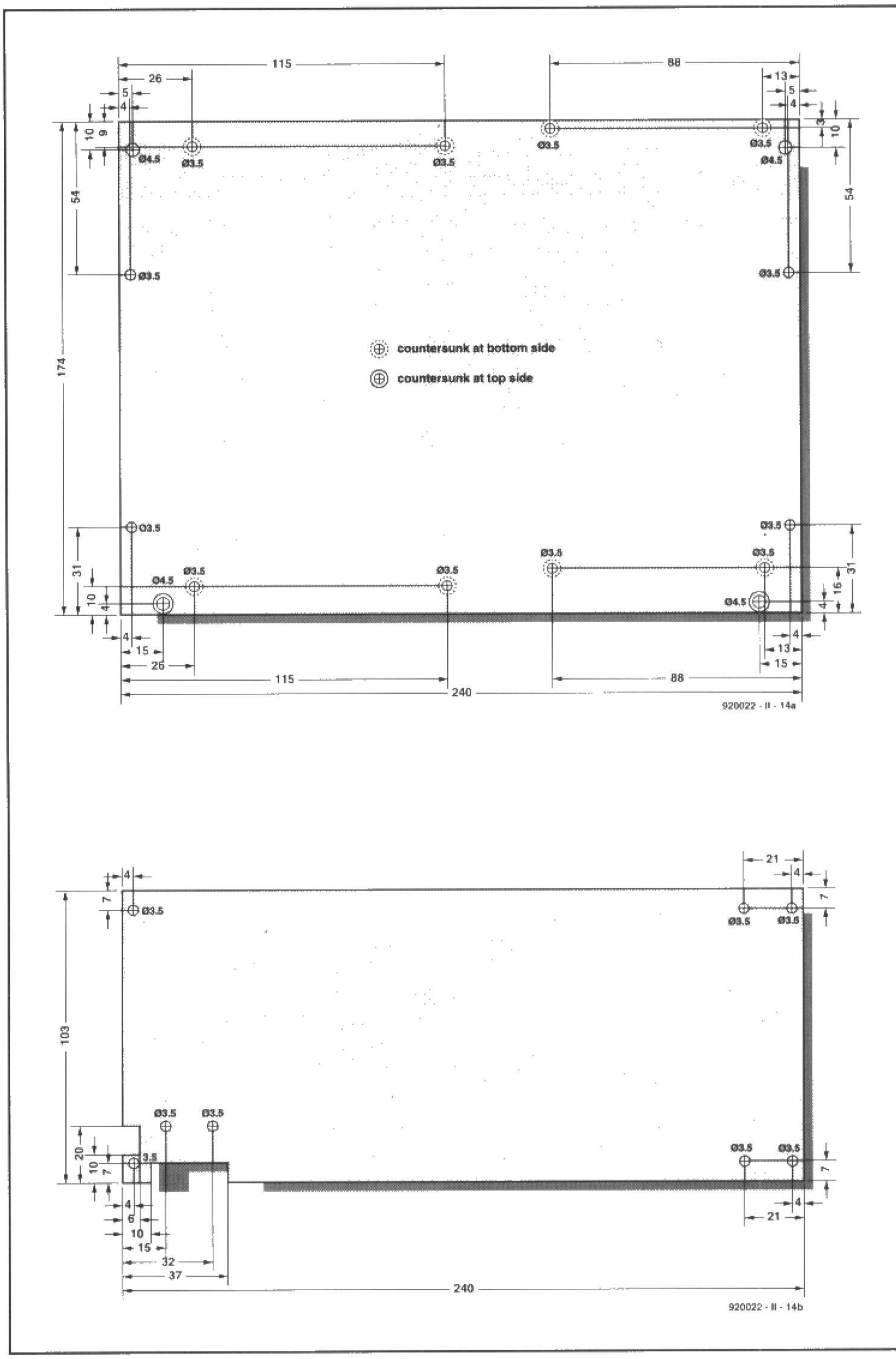


Fig. 32. Drilling details of the two mounting plates in the enclosure.

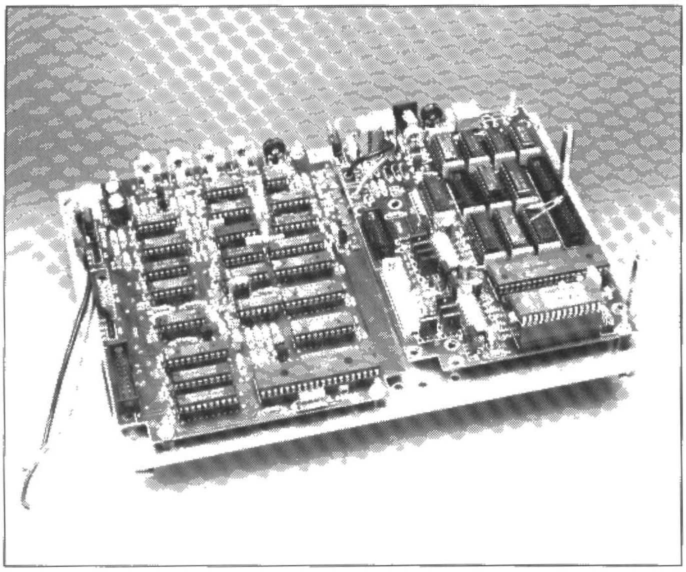


Fig. 33a. The timecode interface and the dissolve unit are fitted on to the bottom plate. Next, the bottom plate is slid into the enclosure.

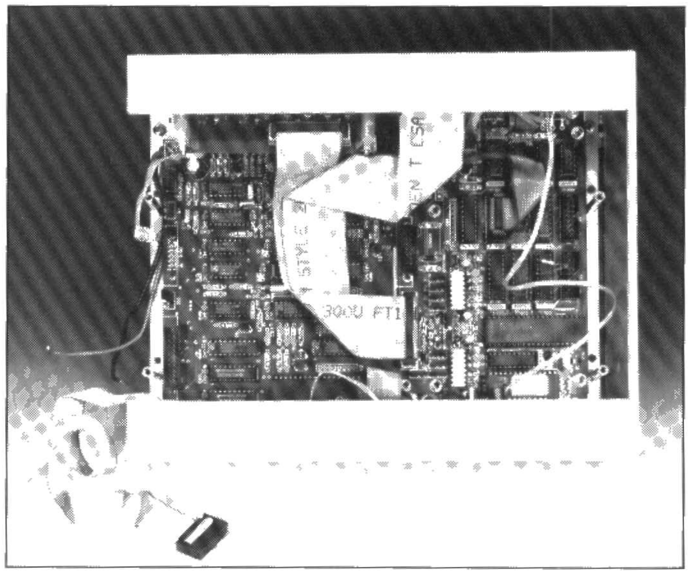


Fig. 33d. Be sure to make all connections underneath the board before mounting the Z80 card on PCB spacers.

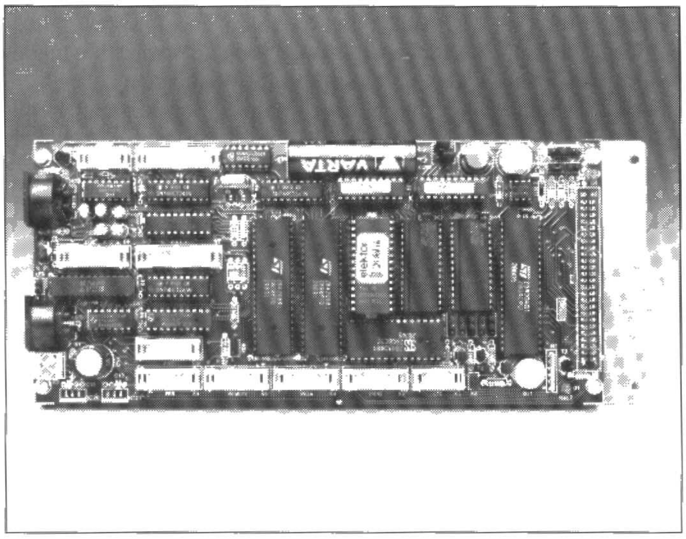


Fig. 33b. The Z80 card is also fitted on an aluminium plate, which also serves as a heat-sink for the voltage regulators.

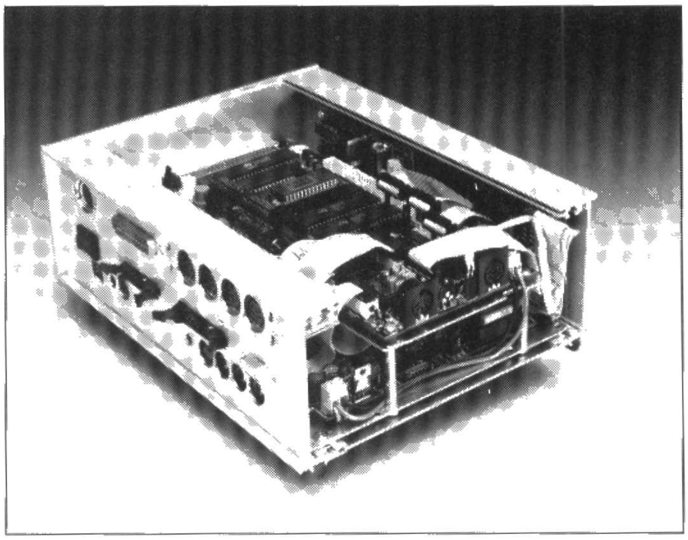


Fig. 33e. The Z80 card is the last module fitted before the side panel can be screwed on.

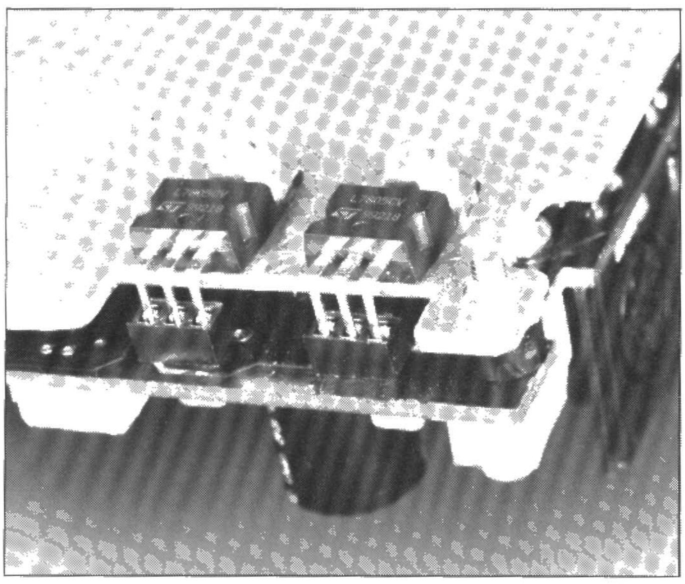


Fig. 33c. The bottom plate used to hold the Z80 card doubles as an excellen heat-sink for the two volatge regulators. As shown here, two pieces of IC socket are used as connectors.

12-V 1.5-A halogen lamp transformer is a perfect a.c. mains adapter. These transformers are now also available with a moulded mains plug.

The EXT1 connection may also be brought out. If it is used to connect a second timecode interface (with LED display), this will be selected at power-on. This allows you to use the external timecode interface at home, for programming purposes, while the 'internal' timecode interface is used 'on location'. To reduce cost, it is, of course, also possible to use the external timecode interface only.

Next time

Next month's instalment will deal with testing the main unit. In addition, we will discuss the control software. The last subject tackled will be the practical use of the DiAV system. To close off, some examples will be given of pulse synchronization and timecode synchronization. ■

ISOLATION AMPLIFIERS

THE SOLUTION TO SOME VEXING INSTRUMENTATION CIRCUIT PROBLEMS

By Joseph J. Carr

MOST solid-state electronic circuits normally operate in a low voltage environment, and may be seriously harmed — even destroyed — in a high voltage circuit. Several such situations come to mind quickly. One example is the analogue section of a computerized power mains monitor system. These circuits measure the AC voltage and current, and then pass the data to a computer. Regardless of where the system is used, it will be at a relatively high voltage compared to other electronic circuits (120 and 240 V_{rms} being common values). Another application is measuring the temperature of an electric furnace using a thermocouple. The list could go on and on. In those circuits where it is necessary to operate a device at a high voltage potential, the solution may well be the isolation amplifier.

There are also many situations where the issue is the safety of a human, rather the safety of the circuit. In medical electronics, where sensors or electrodes of various types must be connected to patients, the supporting circuits must be designed in a manner that does not lead to inadvertent electrical hazards. Small 'microshock' currents, not ordinarily perceptible, are believed to be dangerous to certain patients when their skin is pierced with electrical conductors. The danger level for ordinary electrical situations (with skin intact) is relatively large (100 to 300 mA); in cases where the skin is breached the danger level is considerably lower.

Although some controversy exists about the actual dangerous level, the normal maximum safe level from 50/60 Hz alternating current (AC) is generally set at 10 μA [1]. When designing sensors or sensor electronics for this environment it is therefore necessary to keep AC power mains leakage levels in the instrument very low. The high-voltage transients from defibrillators used in emergency medical procedures can severely damage electronic instruments such as ECG preamplifiers [2]. The usual method for accomplishing the safety goals for both patients and equipment is to use an isolation amplifier for the input stage of the electronics package used with sensors.

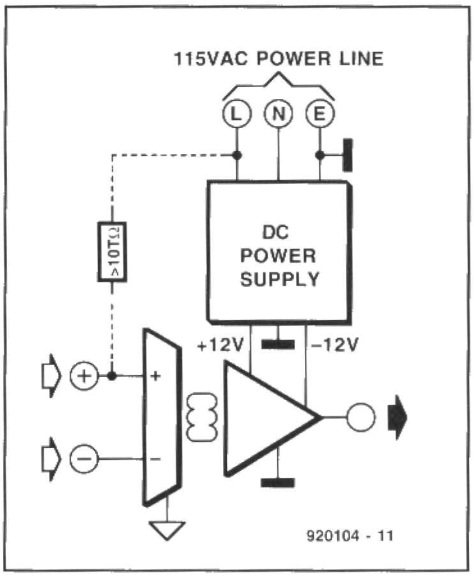


Fig. 1. Block diagram of a typical isolation amplifier.

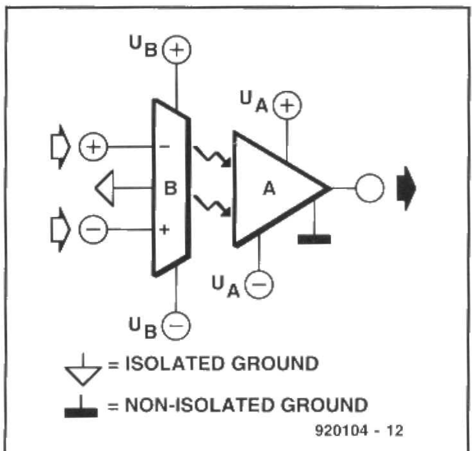


Fig. 2. Circuit symbol for the isolation amplifier.

Isolation amplifiers

So what is an isolation amplifier? An isolation amplifier (Fig. 1) is an amplifier that has an extremely high impedance between the signal inputs and its main DC power supply terminals. These terminals are usually connected to a DC power supply that is, in turn, connected to the AC power mains. Thus, in isolation amplifiers there is an extremely high resistance (of the order of $>10^{12}$ ohms) between the amplifier input terminals and the AC power mains. Modern isolation amplifiers can provide more than 10^{12} ohms of isolation between the AC power mains and the signal inputs so are suitable for all classes of problem discussed above.

Several different circuit symbols are used to denote the isolation amplifier in electronic schematic diagrams, but the one that is the most common is shown in Fig. 2. It consists of the regular triangular amplifier symbol broken in the middle to indicate isolation between the 'A' and 'B' sections. The following connections are usually found on the isolation amplifier:

- Non-isolated 'A' side: $U+$ and $U-$ DC power supply lines (to be connected to a DC supply powered by the AC mains), output to the rest of the (non-isolated) circuitry, and (in some designs) a non-isolated ground or common. This ground is connected to the chassis or main system ground also served by the main DC power supplies.
- Isolated 'B' side: isolated $U+$ and $U-$, isolated ground or common and the signal inputs. The isolated power supply and ground are not connected to the main power supply or ground systems. Batteries are sometimes used

for the isolated side, while in other cases special isolated DC power supplies derived from the main supplies are used (of which, more later).

It is the customary practice to use two different ground symbols for isolated and non-isolated ground connections. The isolated ground is a counterpoise, or floating, ground, while the non-isolated ground can be either a counterpoise ground or a chassis ground.

Approaches to isolation amplifier design

Different manufacturers use different approaches to the design of isolation amplifiers, and some of these are relatively easy for hobbyists to duplicate. Common circuit approaches to isolation include: battery power, carrier operated, optically coupled, and current loading. These methods are discussed in detail below.

Battery powered isolation amplifiers

The battery approach to isolation amplifier design is perhaps the simplest to implement, but it is not always most suitable owing to problems inherent in battery upkeep. A few products exist, however, that use a battery-powered front-end amplifier, even though the remainder of the equipment is powered from the AC power mains. Other products are entirely battery powered. A battery powered amplifier or instrument is isolated from the AC power mains only if the battery is disconnected from the charging circuit during use. In some battery powered instruments used in medicine, mechanical interlocks and electrical logic circuitry prevent the instrument from being turned on if the AC power cord is still attached.

Carrier operated isolation amplifiers

Figure 3a shows an isolation amplifier that uses the carrier signal technique to provide isolation. The circuitry inside the dashed line is isolated from the AC power mains (in other words, the 'B' side of Fig. 2). The voltage gain of the isolated section is typically in the range ×1 to ×500 depending on application.

The isolation is provided by separation of the ground, power supply and signal paths into two mutually exclusive sections by high frequency transformers Tr1 and Tr2. These transformers have a design and core material that works very well in the ultrasonic (20 kHz to 500 kHz) region, but is very inefficient at the 50/60 Hz frequency used by the AC power mains. This design feature allows the transformers to easily pass the high frequency carrier signal, while severely attenuating 50/60 Hz energy. Although most models use a carrier frequency in the 50 kHz to 60 kHz range, examples of

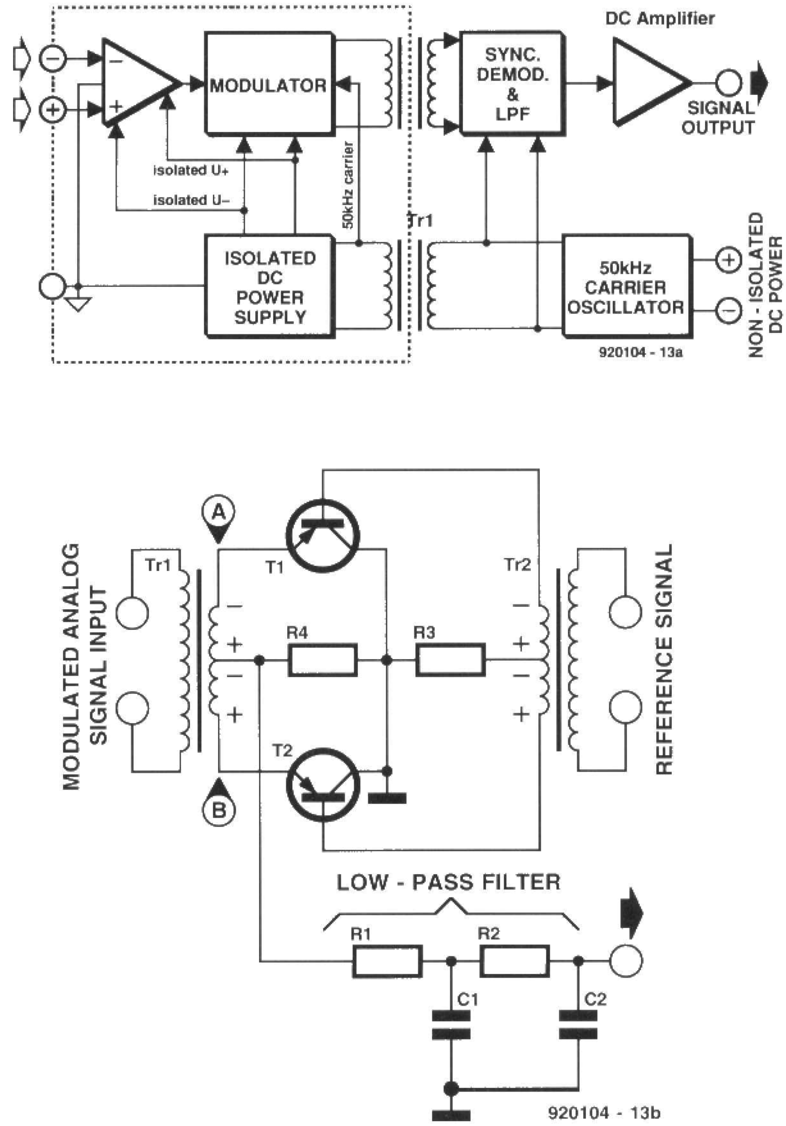


Fig. 3. a) Carrier type isolation amplifier; b) phase sensitive detector circuit.

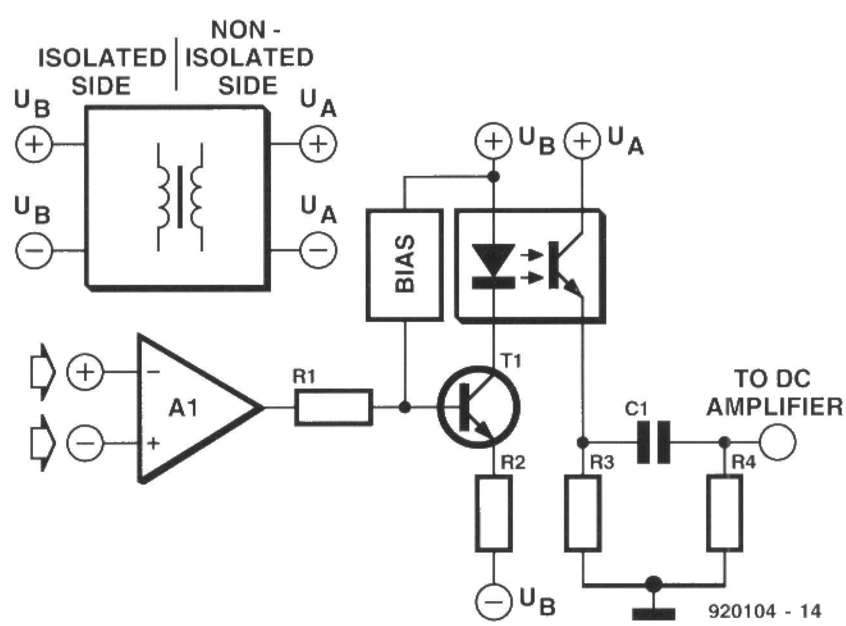


Fig. 4. Direct optically coupled isolation amplifier.

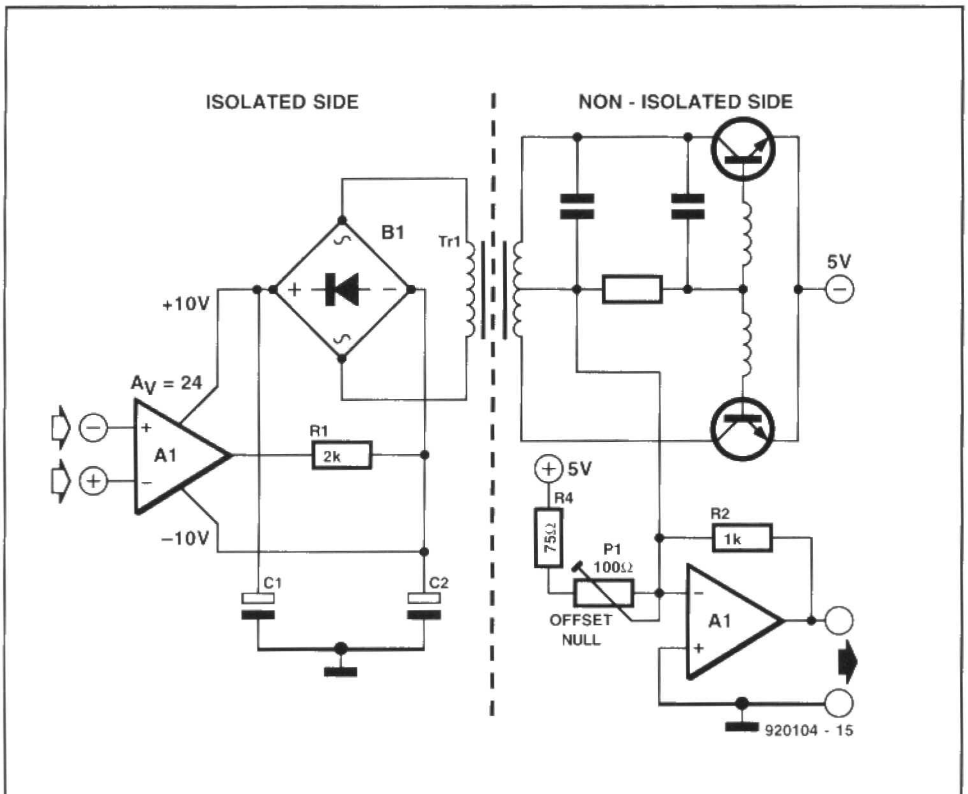


Fig. 5. Current-loading isolation amplifier.

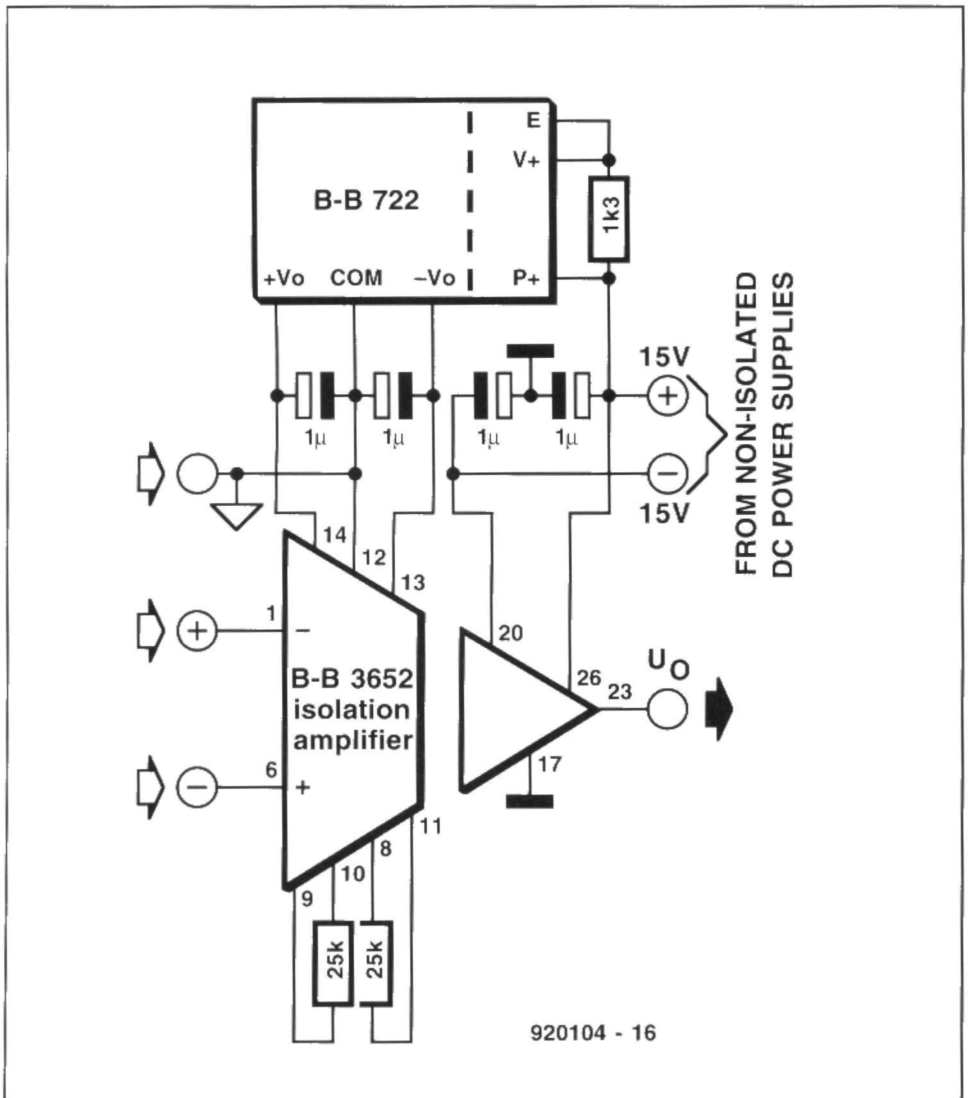


Fig. 6. Practical isolation amplifier.

carrier amplifiers exist over the entire 20 kHz to 500 kHz range.

The carrier oscillator signal is coupled through transformer Tr1 to the isolated stages. Part of the energy from the secondary of Tr1 is directed to the modulator stage; the remainder of the energy is rectified and filtered, and then used as an isolated DC power supply. The DC output of this power supply is used to power the input 'B' amplifiers and the modulator stage.

An analogue signal applied to the input is amplified by A1, and is then applied to one input of the modulator stage. This stage amplitude modulates the signal on to the carrier. Transformer Tr2 couples the signal to the input of the demodulator stage on the non-isolated side of the circuit. Either envelope or synchronous demodulation may be used, although the latter is considered superior. Part of the demodulator stage is a low-pass filter that removes any residual carrier signal from the output signal.

Ordinary DC amplifiers following the demodulator complete the signal processing chain.

An example of a synchronous demodulator circuit is shown in Fig. 3b. These circuits are based on switching action. Although the example shown uses bipolar p-n-p transistors as the electronic switches, other circuits use n-p-n transistors, FETs or CMOS electronic switches (e.g., 4066 device).

The signal from the modulator has a fixed frequency in the range from 20 kHz to 500 kHz, and is amplitude modulated with the input signal from the isolated amplifier. This signal is applied to the emitters of transistors T1 and T2 (via Tr1) in push-pull. On one-half of the cycle, therefore, the emitter of T1 will be positive with respect to the emitter of T2. On alternate half-cycles, the opposite situation occurs: T2 is positive with respect to T1. The bases of T1 and T2 are also driven in push-pull, but by the carrier signal (called here the 'reference signal').

This action causes transistors T1 and T2 to switch on and off out of phase with each other.

On one half of the cycle, the polarities are as shown in Fig. 3b; transistor T1 is turned on. In this condition, point 'A' on Tr1 is grounded. The voltage developed across load resistor R4 is positive with respect to ground.

On the alternate half-cycle, T2 is turned on, so point 'B' is grounded. But the polarities have reversed, so the polarity of the voltage developed across R4 is still positive. This causes a full-wave output waveform across R4, which when low-pass filtered becomes a DC voltage level proportional to the amplitude of the input signal. This same description of synchronous demodulators also applies to the circuits used in some carrier amplifiers (a specialized laboratory amplifier used for low-level signals).

A variation on this circuit replaces the modulator with a voltage controlled oscillator (VCO) that allows the analogue signal to frequency modulate (FM) a carrier signal generated by the VCO.

The power supply carrier signal is still required, however. A phase detector, phase-locked loop (PLL), or pulse-counting FM detector on the non-isolated side recovers the signal.

Optically coupled isolation amplifier circuits

Electronic optocouplers (also called optoisolators) are sometimes used to provide the desired isolation. In early designs of this class, a light emitting diode (LED) was mounted together with a photoresistor or phototransistor. Modern designs, however, use integrated circuit (IC) optoisolators that contain an LED and a phototransistor inside a single DIP IC package.

There are actually several approaches to optical coupling. Two common methods are the carrier and direct methods. The carrier method is the same as discussed in the previous section, except that an optoisolator replaces transformer Tr2. The carrier method is not the most widespread in optically coupled isolation amplifiers because of the frequency response limitations of some IC optoisolators. Only recently have these problems been resolved.

The more common direct approach is shown in Fig. 4. This circuit uses the same DC-to-DC converter to power the isolated stages as was used in other designs. It keeps A1 isolated from the AC power mains but is not used in the signal coupling process. In some designs, the high frequency 'carrier' power supply is actually a block separate from the isolation amplifier.

The LED in the optoisolator is driven by the output of isolated amplifier A1. Transistor T1 serves as a series switch to vary the light output of the LED proportional to the analogue signal from A1.

Transistor T1 normally passes sufficient collector current to bias the LED into a linear portion of its operating curve. The output of the phototransistor is AC coupled to the remaining amplifiers on the non-isolated side of the circuit, so that the offset condition created by the LED bias is eliminated.

Although not strictly speaking an isolated amplifier by the definition used herein, there is another category of optical isolation that is especially attractive for applications where the environment is too hostile for ordinary electronics. It is possible to use LED and phototransistor transmitter and receiver modules in a fibre optic system to provide isolation. A battery powered (or otherwise isolated) amplifier will sense the desired signal, convert to an AM or FM light signal, and transmit it down a length of fibre optic cable to a phototransistor receiver module. At that point the signal will be recovered and processed by the non-isolated electronics.

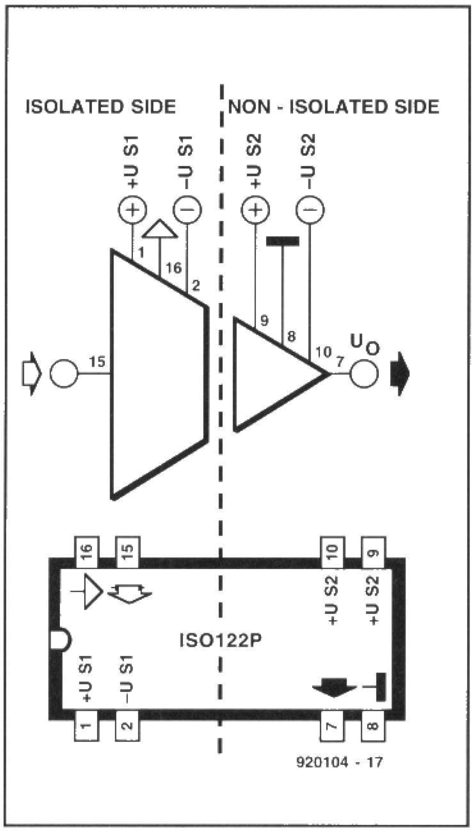


Fig. 7. ISO122P circuit diagram and pinouts.

Current loading isolation amplifier methods

A unique 'current loading' isolation amplifier was used in the front end of an electrocardiograph (ECG) medical monitor. A simplified schematic is shown in Fig. 5. Notice that there is no obvious coupling path for the signal between the isolated and non-isolated sides of the circuit. The gain-of-24 isolated input preamplifier (A1) in Fig. 5 consists of a high input impedance operational amplifier. This amplifier is needed in order to interface with the very high source impedance normal to electrodes in ECG systems. The output of A1 is connected to the isolated –10 V power supply through load resistor R1. This power supply is a DC-to-DC converter operating at 250 kHz. Transformer Tr1 provides isolation between the floating power supplies on the isolated 'B' side of the circuit and the non-isolated 'A' side of the circuit (which are AC-line powered).

An input signal causes the output of A1 to vary the current loading of the floating –10 V power supply. Changing the current loading proportional to the analogue input signal causes variation of the Tr1 primary current that is also proportional to the analogue signal. This current variation is converted to a voltage variation by amplifier A2. An offset null control (P1) is provided in the A1 circuit to eliminate the offset at the output due to the quiescent current flowing when the analogue input signal is zero. In that case, the current loading of Tr1 is constant, but still provides an offset to the A2 amplifier.

Commercial product examples

There are several isolation amplifiers on the market in both monolithic integrated circuit and hybrid versions. In this section we will look at two commercial products. You can also experiment using the principles discussed above. The optoelectronic versions are especially amenable to hobbyist design.

Burr-Brown 3652

Figure 6 shows the circuit of an isolation amplifier based on the Burr-Brown 3652 isolation amplifier device. The DC power for both the isolated and non-isolated sections of the 3652 is provided by the 722 dual DC-to-DC converter. This device produces two independent ±15 V supplies that are each isolated from the 50/60 Hz AC power mains and from each other. The 722 device is powered by a +12 V source that is derived from the AC power mains. In some cases, the non-isolated section (which is connected to the output terminal) is powered from a bipolar DC power supply that is derived from the 50/60 Hz AC mains, such as a ±12 V or ±15 V supply. In no instance, however, should the isolated DC power supplies be derived from the AC power mains.

There are two separate ground systems in this circuit, symbolized by the small triangle and the regular 'chassis ground' symbol. The isolated ground is not connected to either the DC power supply ground/common or the chassis ground. It is kept floating at all times, and becomes the signal common for the input signal source.

The gain of the circuit is approximately:

$$A_v = \frac{1{,}000{,}000}{R1 + R2 + 115} \quad . \qquad (1)$$

In most design cases, the issue is the unknown values of the gain setting resistors. We can rearrange equation (1) to solve for (R1 + R2):

$$(R1 + R2) = \frac{1{,}000{,}000 + (115 A_v)}{A_v} [\Omega]. \qquad (2)$$

Where:
R1 and R2 are in ohms (Ω);
A_v is the voltage gain desired.

Burr-Brown ISO122P

The ISO122P device is an isolation amplifier contained in a 16-pin single-wide plastic DIP package. One of the endearing features of the ISO122P is that it provides isolation amplifier functions at a

low cost. According to a recent catalogue, the price in unit quantities is less than \$20. The ISO122P features unity gain, a high isolation mode rejection of 140 dB, and 0.020% non-linearity.

It can be used alone, or in conjunction with other circuitry on either the isolated or non-isolated sides. Figure 7 shows the schematic symbol and the 16-pin DIP enclosure pin designation).

Figure 8 shows a sample application circuit in which the unity gain ISO122P is used as an output buffer between a DC differential amplifier and the rest of the circuit. The DC differential amplifier is shown here as an example only, and can be replaced with any circuit of your choice provided that the ±10 V input voltage range of the ISO122P is not exceeded.

If the input circuit of Fig. 8 is used, then the operational amplifier at A1 can be a 741, CA-3140 or any other that serves the purpose. The pin-outs shown for A1 are 'industry standard' for a wide variety of devices, including the 741 and CA-3140 devices. If $R_1=R_2$, and $R_3=R_4$, then the differential voltage gain of the circuit of Fig. 8 is given by:

$$A_{vd} = \frac{R_3}{R_1} = \frac{R_4}{R_2} \quad . \tag{3}$$

The power for the isolated side of the ISO122P is shown in the form of a DC-to-DC converter, of which the B-B 722 shown earlier is but one example. Alternatively, one could use batteries for the isolated side, and then ensure that they are charged through some circuit, such as an electromechanical relay, that does not destroy the isolation feature.

Two sets of bypass capacitors are shown on the isolated side, and one set on the non-isolated side. These capacitors should be positioned as close as possible to the pins on A_1 and A_2 that they serve. Otherwise, oscillations and other problems can result.

Conclusion

Although the isolation amplifier is considerably more expensive than common IC linear amplifiers, there are applications where these amplifiers are absolutely esential. Wherever the instrument could cause injury to a human, or wherever the environment is such that the electronics must be isolated for its own sake, the isolation amplifier is the device of choice (at least in the front-end).

The isolation amplifier is generally the solution of choice for most engineers who must interface sensors under conditions that could potentially be dangerous. In addition, they are also the solution of choice for the case where the amplifier input circuits are sometimes subjected to high voltages, either transient or steady-state. ■

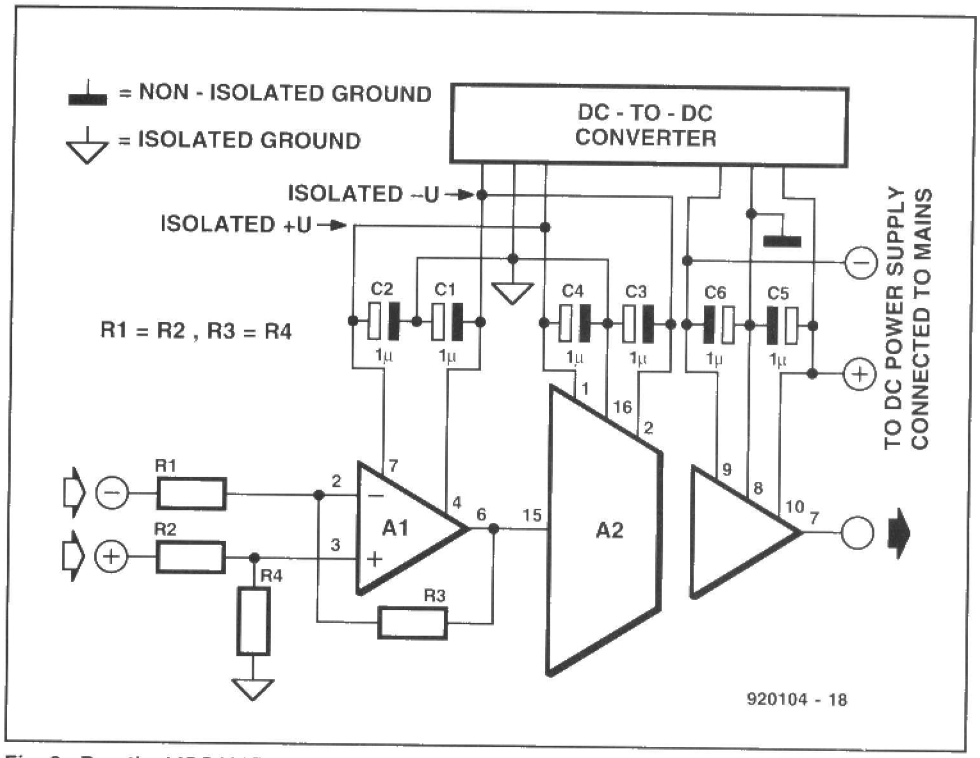
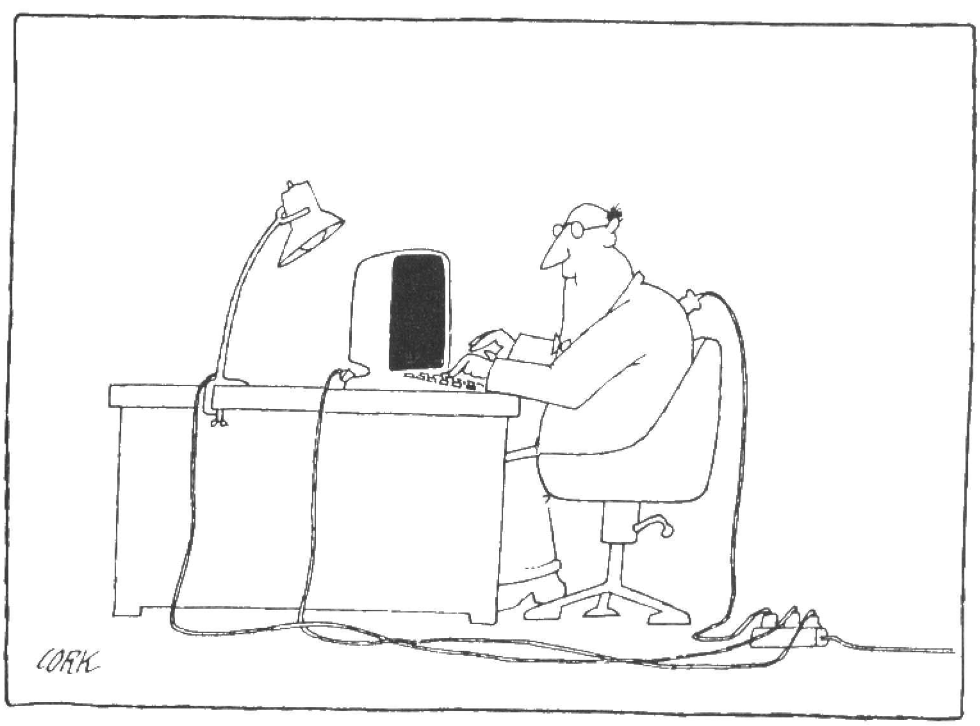


Fig. 8. Practical ISO122P circuit.

References and notes

1. John M. Brown and Joseph J. Carr, *Introduction to biomedical equipment technology*, John Wiley & Sons (New York, 1981); *Patient safety — Electrical safety*, Hewlett-Packard applications note AN-718 (Waltham, MA 1971); *Using electrically monitored cardiac patient*, Hewlett-Packard applications note AN-735 (Waltham, MA 1970); *AAMI safety standards for electromedical apparatus, safe current limits*, Association For the Advancement of Medical Instrumentation (Arlington, VA 1977).

2. The defibrillator is a high-voltage capacitor discharge device used to shock the heart out of a fatal arrhythmia called *ventricular fibrillation*. In the classic Lown machine, the voltage applied to the patient's chest, in close proximity to ECG electrodes and blood pressure sensors, can reach about 3,000 V.



COOKING TIMER

If only poor King Alfred had used a cooking timer, he might not have burnt his cakes in the oven! Unfortunately, with today's Three-Jobs-At-Once type housewives, similar gastronomic catastrophes can easily occur in these modern times too. That is why many kitchens boast mechanical timers to remind the cook that it is time to put the peas on to boil.

By Chris Brown

HOWEVER, mechanical timers usually only produce a feeble, metallic, 'ping' sound when the slotted time has elapsed. Plus, owing to the pointer slowly unwinding back to zero, you can not see how long a certain item has been cooking. On the electronic version, a buzzer sounds until reset by the user. It also shows the total cooking time, and the time elapsed so far. Another advantage is that it can time as little as thirty seconds; mechanical timers can be very fickle about trying to set such small time spans with any degree of accuracy.

The timer consists of three ICs, a handful of discrete components, and a set of LEDs to provide a readout. There is also a rotary switch to dial in the required cooking time, and a couple of push-buttons to mute the buzzer and restart the timer.

The LEDs are arranged in a circle around the time setting switch. Thus, if the cook wanted to roast some chops for, say, 35 minutes, he or she would set the pointer to the 9 o'clock position. After 5 minutes, the LED at the 5 min. position would light, followed, five minutes later, by the 10 min. LED, and so on, until the 35 min. LED lights, whereupon the buzzer will sound.

After some probing, smelling and tasting, Chef decides a further 10 minutes are needed, so he moves the pointer to the ten-minute mark at the 2 o'clock position. Next, he presses the RESTART button. Minutes and half minutes can also be timed by watching four extra LEDs, although these will not sound the buzzer.

Circuit description

At the heart of the circuit is a Type 555 timer, set up to produce a low-to-high transition every thirty seconds. When the device is switched on, the output of IC1 goes high for about 20 seconds. It then goes low for about 10 seconds, whereupon it swings high again, and so on. These low-to-high pulses clock IC2, a Type 4017 counter/divider with ten separate outputs.

Output 0 of this IC is connected to a further counter, IC3, also a 4017. This

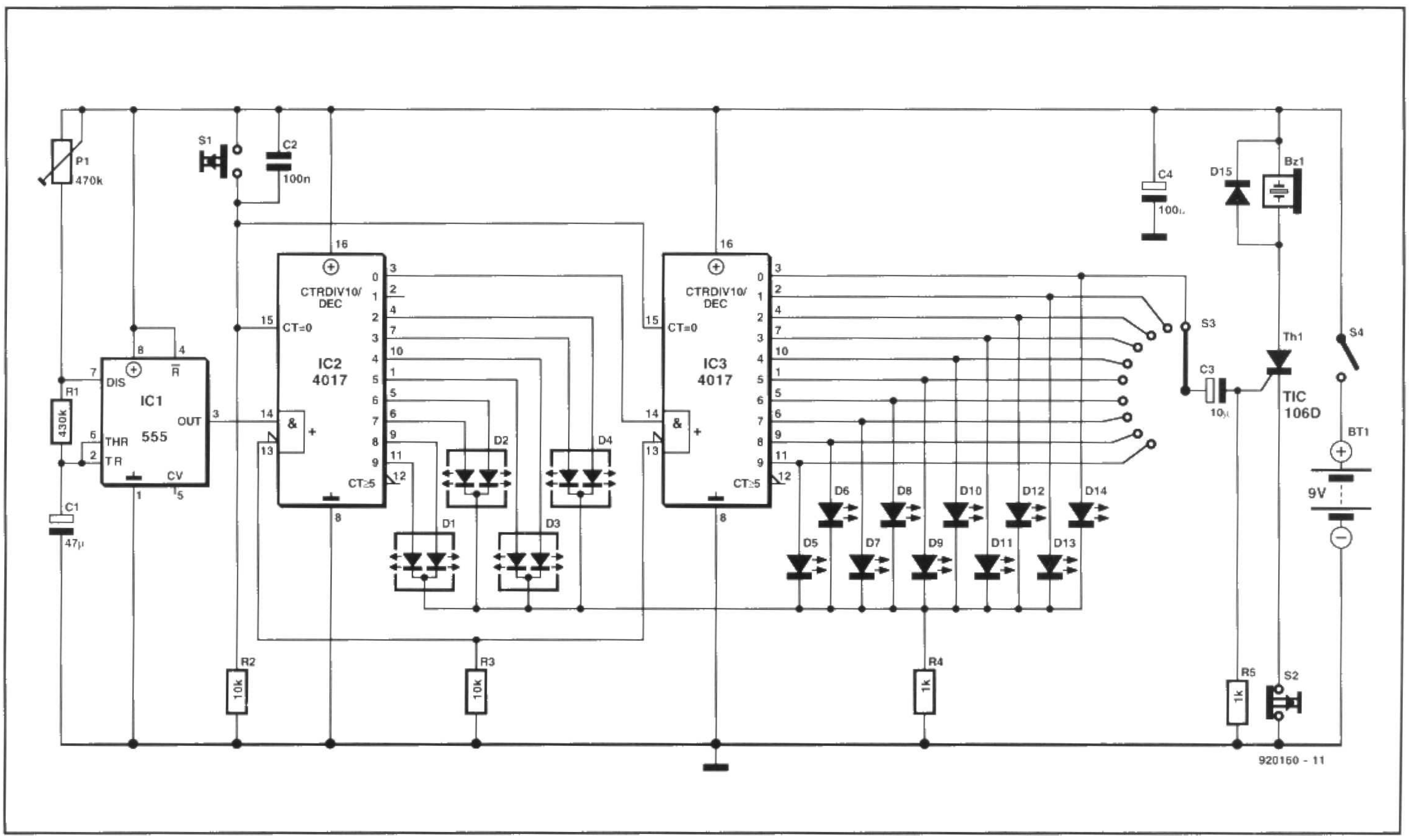


Fig. 1. Circuit diagram of the cooking timer.

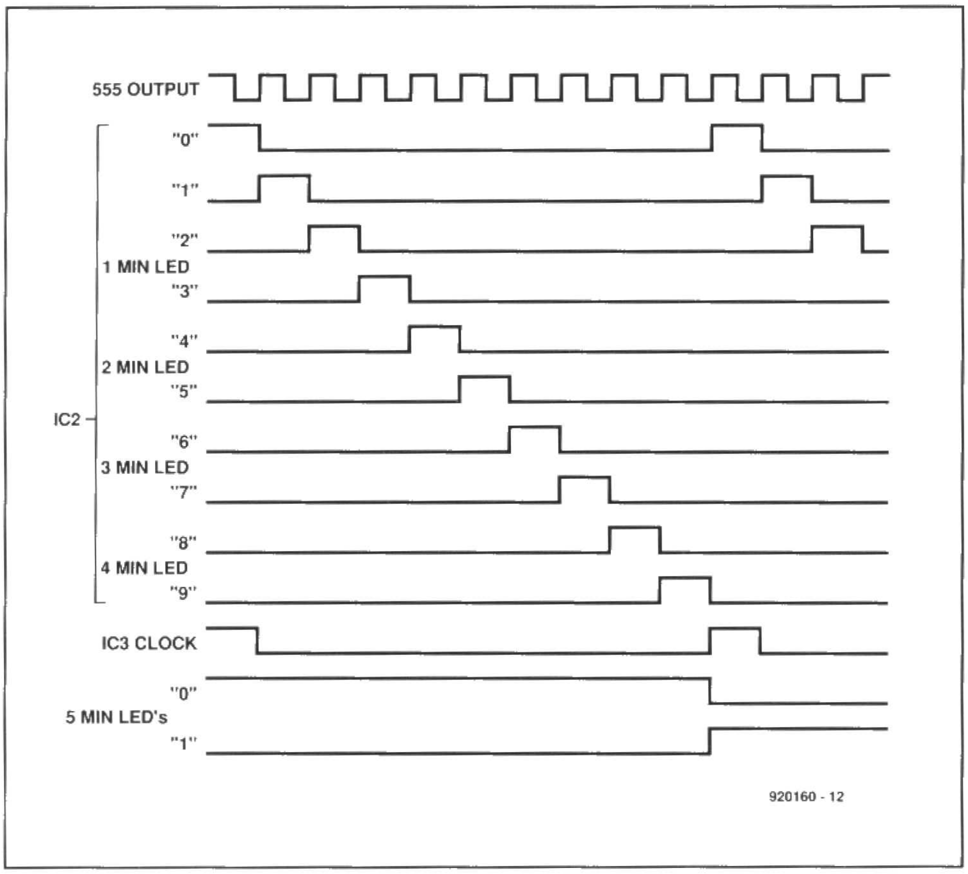


Fig. 2. Timing diagram to illustrate the operation of the circuit. Two squares equal 30 seconds.

output is high when the circuit is first switched on, but swings low when output 1 goes high upon the next clock pulse supplied by the 555. Thirty seconds later, another clock pulse arrives, and output 2 swings high, which illuminates the first bi-colour LED to indicate that 1 minute has elapsed.

Output 4 lights the second bi-colour LED, and so on, until output 8.

After two more clock pulses, output 0 goes high again, the low-to-high transition clocking IC3, and making its output 1 swing high. This lights the LED at the 5-min. position. Again, the bi-colour LEDs light to indicate 6 mins. (5 mins. plus 1 min.), 7 min (5 min. plus 2 min.), 8 min and 9 min. On the tenth minute, the second LED comes on at the 2 o'clock position. The timing of the ICs is illustrated in Fig. 2.

All the red LEDs, (5 min., 10 min., etc.) are also connected to a 12-way rotary switch, the common pin being connected to a thyristor via C3. When the selected time LED lights, C3 partially discharges via R5, and partially through the thyristor's gate terminal. The thyristor 'fires', and the sounder is energized via switch S2. When this is pressed, the thyristor looses holding current, so that the buzzer is muted. Push-button S1 is connected to the reset inputs of the two 4017s. Taking these high resets both counters, so that both '0' outputs go high. At switch-on, C2 discharges via R2, which has a similar effect.

Construction

The case is the hardest part to lay out neatly, since the pointer knob fitted on the spindle of the rotary switch has to point at each LED. To create a template, start by bending all the switch contacts out flat, including the middle common pin. Lay the switch on a piece of paper, and mark where each contact is. Draw through each diametrically opposed point to create a 12-point star (Fig. 3). This will give you the approximate centre of the switch. From here, use a compass to draw a circle at a radius where the LEDs will appear. Mark off the 5-50 min. points. Mark the case using this guide, and drill it to accept the LEDs and the rotary switch. Drill the remaining holes for the push switches and the buzzer as shown in Fig. 5.

Alter the rotary switch's stop beneath the locking nut, so that only 11 positions function. Insert the 10 red LEDs so that the anodes are nearest the switch contacts. Carefully bend the wires, and solder them to the contacts. The outer cathodes are now twisted in such a way as to create a ring around the outside. Solder the other components to these again, as illustrated in Fig. 4. The ICs and their surrounding parts may be mounted on a printed circuit board etched for the occasion, or on a piece of stripboard. Since very low frequencies are involved, the layout will not be critical.

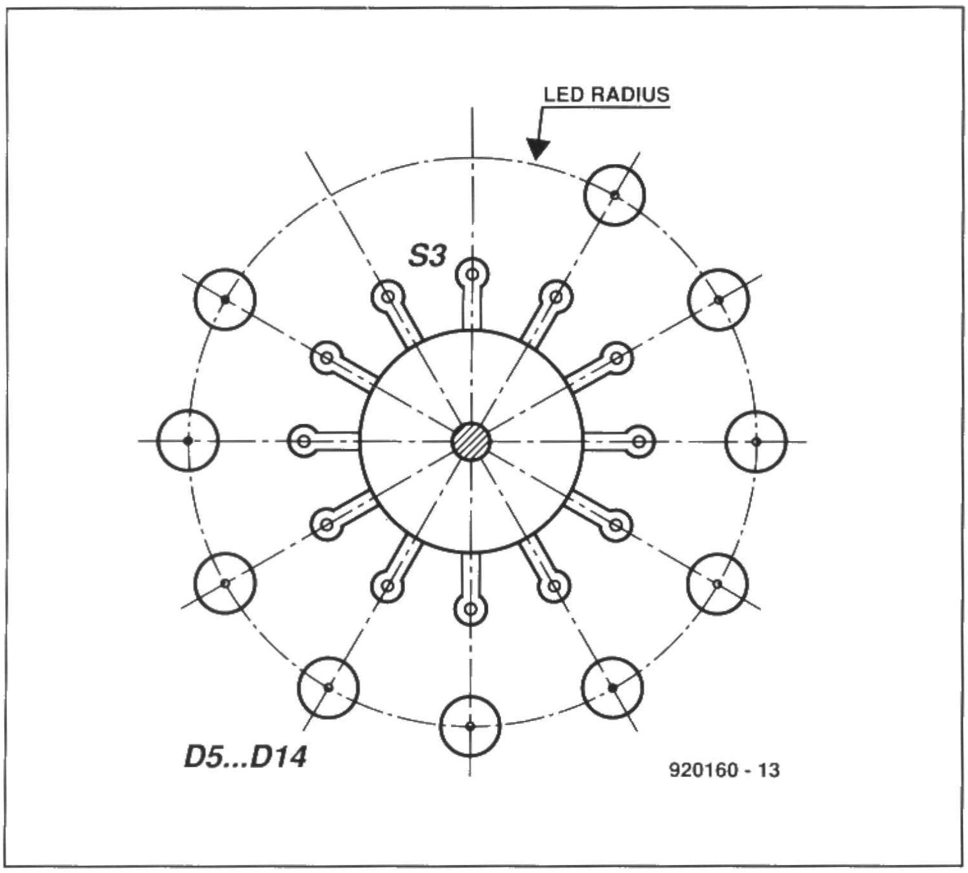


Fig. 3. Marking off the LED locations on the front panel of the timer.

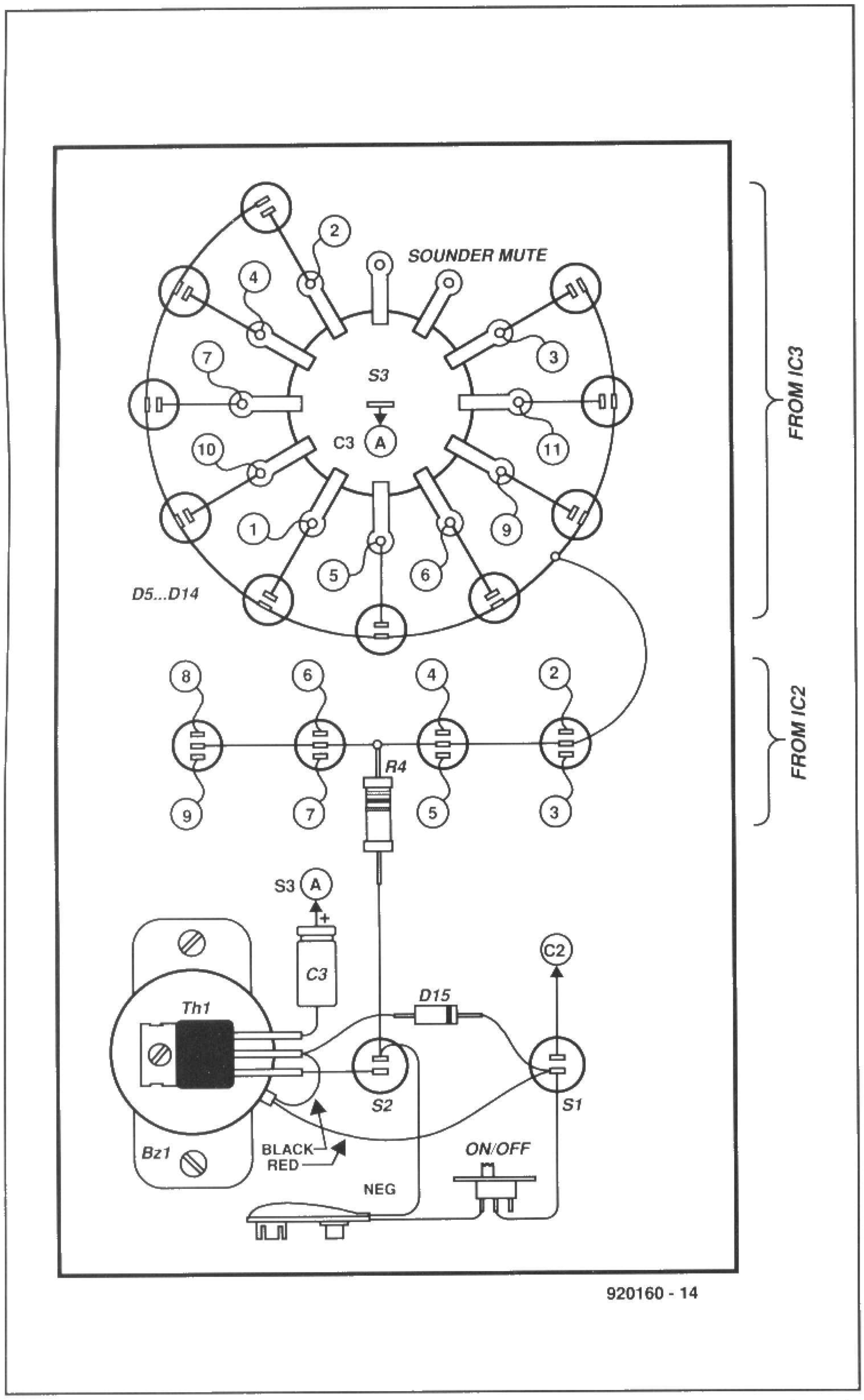


Fig. 4. Case layout seen from inside. The numbers in circles refer to IC outputs (not pin numbers!). The thyristor is bolted to one of the PCB posts used to secure the buzzer.

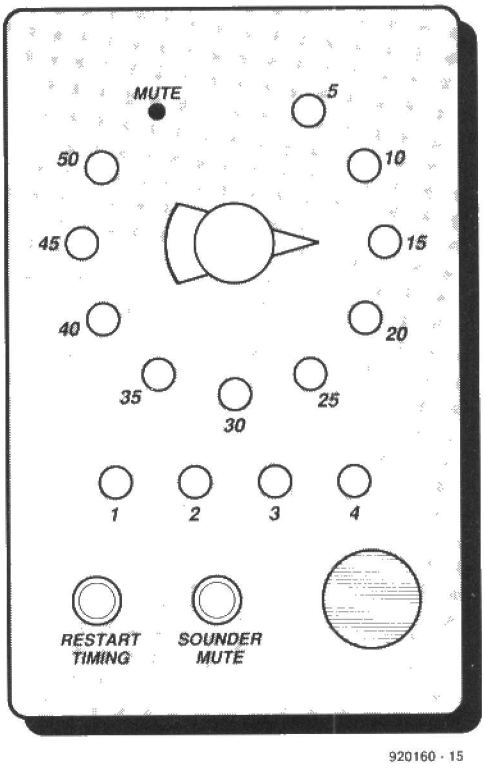


Fig. 5. Suggested front panel layout.

Setting up

Connect the anode of a LED to terminal 3 of IC1, and the cathode to ground. Insert the battery, and wait for the LED to go out. Start your stopwatch as soon as the LED lights again. Ignore it when it goes out, but be ready to stop the clock as soon as it lights again. You have now timed one clock pulse, i.e., from one low-to-high transition to the next. This should be set to 30 seconds as accurately as possible with the aid of potentiometer (or preset) P1. Once set, trim out the test LED connections.

Switches

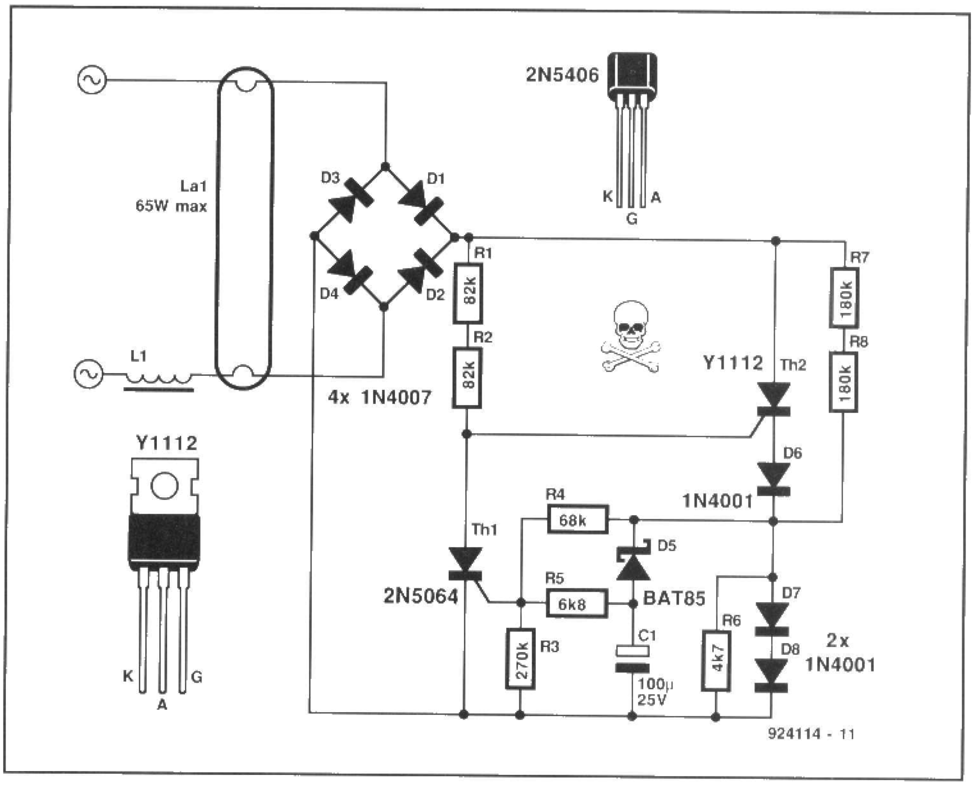
A normal on/off switch can be used, or for a bit of extra ingenuity, a mercury tilt switch. Actually, the latter is easy to make using a piece of Biro tube, sealed one end, with two contacts at the other end. Some water inside the tube will turn the timer on whenever the water bridges the contacts. In this way, the device is switched off when it is laid down, and switched on when held upright.

One position of the rotary switch is left unconnected. This allows you to use the timer as a visual reminder only, without noise being made each time. Note: since there is no sound created, you could put the device away switched on, and it will never 'call' you to tell you it is still operational.

Since most cooks do not require split second precision, the bi-colour LEDs could be deemed as 'greater than 1 min.', 'greater than 2 mins.', etc., irrespective of whether the LED is red or green. However, as shown in the timing diagram, when the LED changes colour, that is an indication that an extra half second has elapsed.

Finally, at switch-on, the 50-min. LED lights, since it is wired to output 0 of the second 4017. If the rotary switch is also set to 50 mins., the buzzer will sound. To mute it, simply press the switch. The buzzer will sound again once the device has timed the next 50 minutes. ■

THYRISTOR STARTER FOR FLUORESCENT TUBES



The Type Y1112 fluoractor™ from Texas Instruments is a specially designed thyristor for starting fluorescent tubes. Its main advantages over a standard thyristor are its much greater hold current, its ability to cope with rapidly rising anode-cathode voltages (high du/dt value), and its overvoltage protection. These properties make it very suitable for replacing a traditional electro-mechanical starter for reliable flicker-free starting and a long life.

A fluorescent tube does not switch on as easily as an incandescent lamp because it can only start at a voltage much higher than the mains, after which it will remain lit at the mains voltage. The level of both the starting voltage and the working voltage depends on the temperature of the tube.

Normally, the high starting voltage is obtained by interrupting the current through a choke. This is usually done by the starter, which also ensures that a fairly large current flows through the filaments of the tube. This heats the ends of the tube, which makes starting easier.

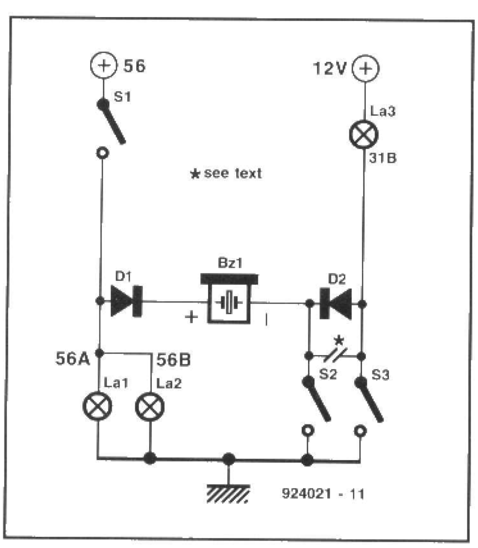
These tasks of the starter are taken over by the fluoractor™, Th_2. When the mains is switched on, Th_2 will start via R_1 and R_2. A fairly large current will then flow through the filaments of the tube so that this will be preheated.

Because of the potential drop across diodes D_7 and D_8, capacitor C_1 is charged via resistors R_4 and R_5. When, after a few milliseconds, the voltage across C_1 has reached a certain value (during which time the current through Th_2 is appreciably larger than the hold current), thyristor Th_1 is switched on, whereupon the gate current of Th_2 is interrupted*. The sudden discontinuation of this fairly large current causes the choke to produce a back-e.m.f. that is high enough to start the fluorescent tube.

(Texas Application – 924114)

*This special thyristor remains on, however, until the current through it has dropped to the hold value of about 200 mA.

CAR LIGHTS WHISTLE BLOWER



Virtually all modern cars have a built-in alarm to warn if you have left the lights on when you are getting out of the car. There are, however, thousands of older cars that have no such useful device and their owners might find the present circuit just what they've been waiting for.

The anode of diode D_1 is connected between the lights switch and the lights. The cathode is connected to the 12 V buzzer. The other terminal of the buzzer is connected to one of the door-switch contacts or to terminal 31B of the interior lights cable. When one of the front doors (fitted with a switch, which, in older cars is not always the case with rear doors) is opened while the external car lights are still on, the buzzer sounds.

Note that the circuit allows for only two door switches: S_2 is the driver's door contact and S_3 the front passenger door's contact.

If you don't want the buzzer to be operated by the front passenger door, fit diode D_2 as shown and break the wire between the switches on the two doors.

Note that the circuit is intended only for cars whose door contacts switch the interior lights to earth (which is the case in most cars built in the past 10 years).

Diode D_1 may be a light-duty type such as the 1N4001, but D_2 must be a somewhat heavier-duty type, such as a 1N5401, since it carries the current through the interior lights.

(E. Tienken – 924021)

RFi SCREENING

By Bill Higgins

With the increase in use of radio frequencies, especially in the higher range of the spectrum, designers and manufacturers of complex equipment are adopting techniques to screen their products from Radio Frequency interference—RFi. Along with new EC regulations relating to electroni products on the market, there is a growing awareness of the need for screening.

Readers of *Elektor Electronics* can benefit from the know-how of large companies: this article shows the techniques used, lists factors to be taken into account when RFi is considered, and presents a host of data for those about to embark on RFi screening.

Why screen?

There are four main reasons to consider screening:

a) to protect equipment against unwanted RFi, for instance, when computer data are used or when sensitive electrical measurements are carried out;
b) to prevent interference generating equipment affecting other equipment;
c) to protect the confidentiality of data in systems from being intercepted by non-authorized users;
d) to protect equipment from the effects of large pulses of electromagnetic radiation, for instance, those caused by electrical storms.

Military equipment is a good example of apparatus that needs screening. It has to withstand nuclear radiation, must not allow any important data to be leaked, and must not be affected by jamming.

Materials used for screening

Basically, efficient screening means really placing the equipment in a box made of suitable material with a lid that can be removed when required for maintenance purposes. That places the onus squarely on to the material of the box.

Knitted wire mesh is widely used for screening, as it can be formed easily into the desired shape. The most frequently used materials for knitted mesh are Monel metal (68% nickel, 29% copper, and 3% iron, manganese, silicon and carbon); aluminium; TCS (tin-plated copper-clad steel); and stainless steel. The relative effectiveness of these materials is shown in Table 1.

Manufacturers often supply small samples of their products for test purposes to enable the most suitable material for the task in hand to be ascertained.

Gaskets

Joints between the lid and the box should have a suitable gasket; this also applies to removable panels, access doors, drawers, and so on. Gaskets are made of a wide range of materials and come in many different shapes and sizes. Their function is to fill any gaps or unevenesses in adjoining metal surfaces.
Points to bear in mind are:

1) poor joints affect the overall effectiveness;
2) clean metal-to-metal contact prevents leakage; ensure freedom from corrosion, moisture, ail and paint;
3) always use the smallest possible gasket;
4) ensure adequate compression of the gasket used;
5) be aware of galvanic corrosion and select gaskets accordingly; for instance, aluminium and silver have a high-value difference, which makes for rapid corrosion where they meet.

Figure 1 shows typical gasket resillience pressures.

Mechanical/physical properties

Monel is an alloy that has been directly smelted from natural ores. Its exact proportions vary, but 70% nickel, 27% copper, 2% iron and 1% managnese gives a good idea of its composition. It has good corrosion characteristics and it is close to neutral on the Galvanic scale.

Aluminium. Owing to its high rating on the Galvanic scale and rapidity of oxidization in air, the use of aluminium is limited. It has, nevertheless, the advantage of low density, so it is used where this property is important.

Tin-plated Copper-clad Steel is produced by a drawing process. It consists of steel clad in copper that has been drawn out to make wires, and the whole is tin-plated. The tin-plating improves the steel's resistance to corrosion, while the copper is used for its electrical properties. As the coating can wear or be scratched off, use of TCS is not recommended for applications where the screening could be abrased easily.

Stainless Steel. The RFi performance of this material is similar to that of aluminium, but it is stronger and can resist wear and tear more easily. A grave disadvantage is the corrosive effect of sea water on it.

Galvanic scale

When two dissimilar metals are in contact in an electrolyte, some electron flow takes place. Although in some cases this process is useful, in RFi screening it causes corrosion, especially if there is moisture present. Table 2 lists the electric potential of a number of materials immersed in a salt-water solution together with a saturated calomel (mercury chloride, Hg_2Cl_2) electrode. When selecting pairs of materials, the difference in their potentials should ideally be not greater than 0.3 V for conditions where wet conditions may prevail, or 0.5 V for indoor use where only slight condensation may occur.

Absorption loss

The absorption loss may be calculated from the equation

$$A=0.1315\cdot t\cdot\sqrt{(f\cdot\sigma\cdot\mu)},$$

Freq. (MHz)	Monel	aluminium	TCS	stainless steel
H field	attenuation (dB)			
0.01	54	54	58	54
0.1	63	62	78	64
1.0	75	77	82	72
E field	attenuation (dB)			
1	132	132	132	132
10	114	119	119	115
100	112	124	124	100
1000	97	97	97	89
10000	89	90	90	72

Table 1. Screen effectiveness: typical values.

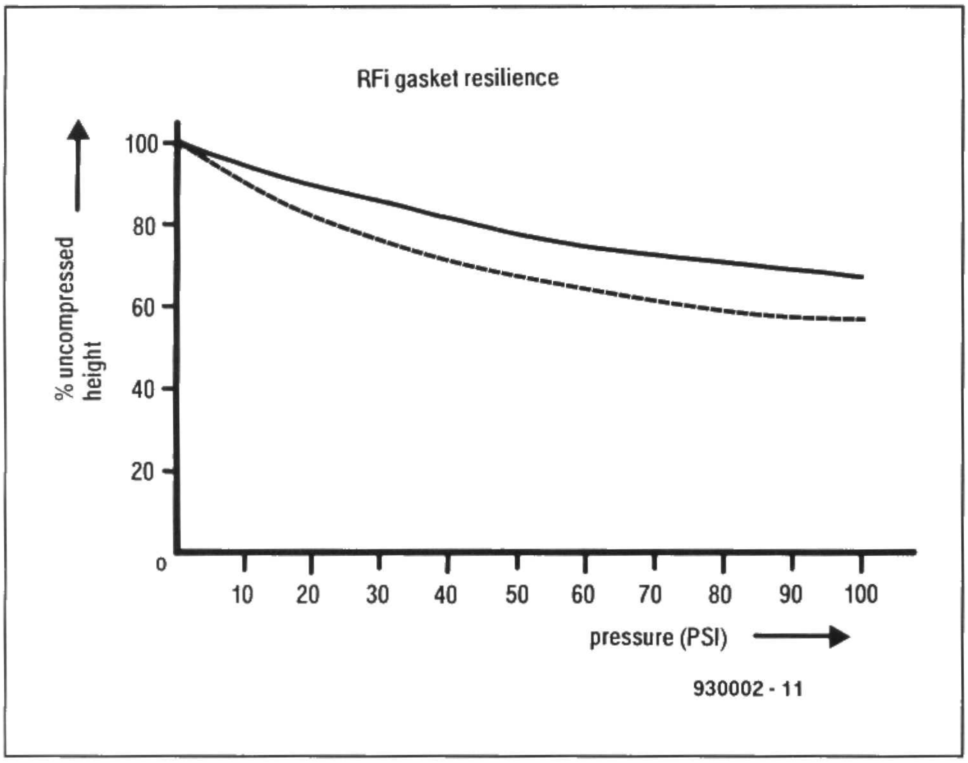


Fig. 1. RFi gasket resilience. Upper curve for all-metal gaskets; lower curve for mesh-covered neoprene.

Platinum	+0.15 V
Gold	+0.15 V
Silver	0 V
Copper	–0.25 V
Copper alloys	–0.25 V
Monel*	–0.25 V
Stainless steel*	–0.45 V
TCS*	–0.5 V
Duralumin	–0.6 V
Aluminium*	–0.75 V
Zinc alloy	–1.1 V

Table. 2. Electric potential of various materials in saturated calomel. Materials with an asterisk are widely used for screening.

Material	μ	σ
Aluminium	1	0.61
Brass	1	0.61
Copper	1	1.00
Monel*	1	0.04
Stainless steel	500	0.02
Tin	1	0.15

Table 3. Conductivity and permeability of various materials relative to copper.

where A is the absorption loss in dB; f is frequency in Hz; t is thickness in mm; σ is conductivity relative to copper; μ is permeability relative to copper. The μ and σ values of several materials are given in Table 3.

The absorption loss of TCS must be assessed from the absorption loss of the steel centre, the copper cladding and the tin plating. As each thickness can vary depending on the drawing process, the calculation can be complex.

For readers of *Elektor Electronics* with personal computers that work in BASIC, the following computer program may be of use:

```
10  PRINT  "Elektor Electronics RFi absorptionloss"
20  PRINT  "Type in frequency under consideration"
30  INPUT  F
40  PRINT  "Type in thickness in mm"
50  INPUT  T
60  PRINT  "Type in conductivity relative to copper"
70  INPUT  0
80  PRINT  "Type in permeability relative to copper"
90  INPUT  U
100 LET A=.1315*T*SQR(F*O*U)
110 PRINT  "Absorption loss in dB is:"
120 PRINT  A "db"
130 END
```

With this program, the absorption loss of 1 mm thick screening made from aluminium, Monel, and stainless steel at various frequencies is found to be:

Material	Frequency 1 kH	1 MHz	1 GHz
	Absorption loss in dB		
Aluminium	3.25	102.7	3247.8
Monel	0.82	26.3	831.7
Stainless steel	13.15	415.9	13150

It can be seen from this table that stainless steel is most suitable for the lower frequencies. With increasing frequency, the absorption loss increases sharply making it difficult for RF signals to penetrate.

Plastics

Where it is not practical to use screen mesh, for instance with equipment that makes extensive use of plastics, other methods are used. One such method is plating on plastic.

Plastic equipment enclosures are coated in such a way that they act as screening for equipment. The process used for this is an electroless form of plating originally developed for plastic Christmas decorations. In this, the cover is immersed in baths of different chemicals so that a coating of copper and nickel is built up on it. Some typical values of shielding effectiveness obtained with this method are given in the table below:

Coating		Frequency	
μm copper	μm nickel	30 MHz	100 MHz
		Effectiveness in dB	
1.0	0.25	70.1	67.9
1.5	0.25	78.1	70.0
2.0	0.25	78.4	73.6

European Community

New regulations regarding permissible levels of electromagnetic radiation from any equipment came into force throughout the EC on 1 January, 1992.

This has a profound effect on the design of electronic equipment: a problem that was until now considered as peculiar to radio apparatus, has become one of general consumer electronic equipment. In other words, such mass market equipment must be screened in the same way as radio equipment.

Summary

RFi screening is used to prevent unwanted r.f. emissions entering or leaving a particular piece of equipment. All electronic designers must now take into account the EC regulations regarding permissible levels of electromagnetic radiation.

Materials used for screening include aluminium, Monel, stainless steel and TCS, in the form of strips, knitted mesh and gaskets. Copper and nickel are used for electroless plating on to plastics.

Galvanic corrosion should be taken into account when selecting screening material.

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PAL test pattern generator (1 × GAL 20V8-25)	**6211**	**9.40**	**16.00**
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FM tuner - 5:			
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